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A Message from the Queen of 3D

Has it already been 10 years since my first business partner, Leo Archer, and I started 3D InCites?

When we first conceived of the idea in 2009, I had no idea what I was getting myself into or that 10 years later, 3D InCItes would be so well recognized in the industry.

Leo and I parted ways in 2011, and in 2012, I partnered with Martijn Pierik and Dave Richardson of Impress Labs (now Kiterocket). Bolstered by the support of these two partners and a web design and development team, I was able to focus on creating valuable content and building a following. I remember how excited I was when, in our first year, we hit 116 registered members. Ten years later, we log in over 80K users annually.

Putting this 10th Anniversary issue together has been a nostalgia trip for me, from searching through the archives and photos, to reading all the contributions from our friends in the industry. For that is how I think of all of you: not just readers, but a community of colleagues.

3D InCites has always been more than just another source of technology news and information. Perhaps Rajiv Roy, FormFactor, said it best in a testimonial: "As a community, 3D InCites brings to life the people, the personalities, and the minds behind 3D integration in a uniquely personal way." It's what sets us apart from the other industry publications, and we live by it. The past 10 years have been full of pivotal moments for the companies and people responsible for developing 3D and heterogeneous integration technologies, and 3D InCites has been lucky to grow up alongside it.

We were there when the EMC3D Consortium put TSVs on the roadmap, and drove cost reduction efforts to bring them to commercialization. We were there when imec, CEA-Leti, SEMATECH, Fraunhofer EMFT, Fraunhofer IZM-ASSID, and others developed back-end processes that are now mainstream.

We were there when companies like Alchimer, ALLVIA, NEXX Systems, Replisaurus, Tezzaron, and Ziptronix were just getting started. We were there for the launches of Deca Technologies, Invensas, KOBUS, and UnitySC. We remember when Alchimer became Aveni, and when Replisaurus went the way of the dinosaurs; and when Ziptronix was acquired by Invensas, and then became Xperi. We remember when Applied Materials and TEL almost became Etaris, and then didn't.

In 2013, we created the 3D InCites Awards to recognize the contributions people, companies, and research institutes have made to bring about the commercialization of 3D and heterogeneous integration technologies. This year marks the 7th year of the awards program. Our statue graces the award cases of Amkor Technology, Inc.; Brewer Science; Bob Patti; Bryan Black; Deca Technologies; Dow Corning (now Dupont); Dusan Petranovic; E-System Design; EV Group; and Fogale Nanotech (now UnitySC); Fraunhofer IZM; Fraunhofer Cluster for 3D Integration; FRT, the Art of Metrology; Gill Fountain; GLOBALFOUNDRIES; KLA; Kobus (now part of PlasmaTherm); imec; Mentor, A Siemens company; OmniVision; Novati Technologies; Paul Enquist; Phil Garrou; Semblant/HZO; SPTS; Sorin CRM; SSEC (now Veeco);TSMC; Xilinx; and Xperi.

Thanks to your sponsorship and donations, we've made significant contributions to the IEEE Women in Engineering Scholarship, SEMI High Tech U, the IMAPS Foundation, G1ve-A-Buck, and Phoenix Children's Hospital.

What does the future hold? 3D integration has finally hit the big time, and we'll continue to bring you the latest developments. Some of them are in this issue. In October 2018, Phil Garrou joined us as a contributing editor, bringing with him his well-known blog, re-christened Packaging InCites from the Leading Edge. He joins Herb Reiter, our EDA expert, as a regular contributor. We've also launched the SemiSister project to support gender diversity and inclusion efforts in the semiconductor industry.

In 2019, the 3D InCites leadership changed again. Dave Richardson has gone on to pursue other interests, leaving Martijn and me at the helm of this particular ship. We are excited for what the next 10 years has in store, and we hope this issue takes you on your own walk down memory lane.

Francoise

Hybrid Bonding: From Concept to Commercialization

By Françoise von Trapp

Hybrid bonding is quickly becoming recognized as the preferred permanent bonding path for forming high-density interconnects in heterogeneous integration applications, from 2.5D to 3D stacking with or without through silicon vias (TSVs), as well as MEMS and III-V applications. In this exclusive interview with Gill Fountain, Xperi, winner of the 2018 3DInCites Engineer of the Year award for his work in this area, we embark on the journey of how one hybrid bonding technology came to be.

What Do We Mean by Hybrid Bonding?

A quick Google search shows that the semiconductor industry has used the term "hybrid bonding" loosely to refer to any alternative to thermocompression bonding that combines metal interconnect with some other form of bonding. In some cases, it includes adhesives, such as work done by imec and its partners, and by a team at Dalian University of Technology in China.[1]

In other cases, it involves various interconnect metals such as copper (Cu), indium (In), and silver (AG). One example is solid-liquid inter-diffusion (SLID) developed by Fraunhofer Institute.[2] Another example is a binary bonding approach that uses InAg combined with atmospheric plasma surface activation, developed by SET-NA.[3]

For the context of this interview, hybrid bonding is defined as a permanent bond that combines a dielectric bond with embedded metal to form interconnections. It's become known industry-wide as direct bond interconnect, or DBI™ (Figure 1).

The early days: developing ZiBond

As Fountain tells it, the DBI story began 20 years ago in the labs at Research Triangle Institute (RTI), when his colleague, Paul Enquist,

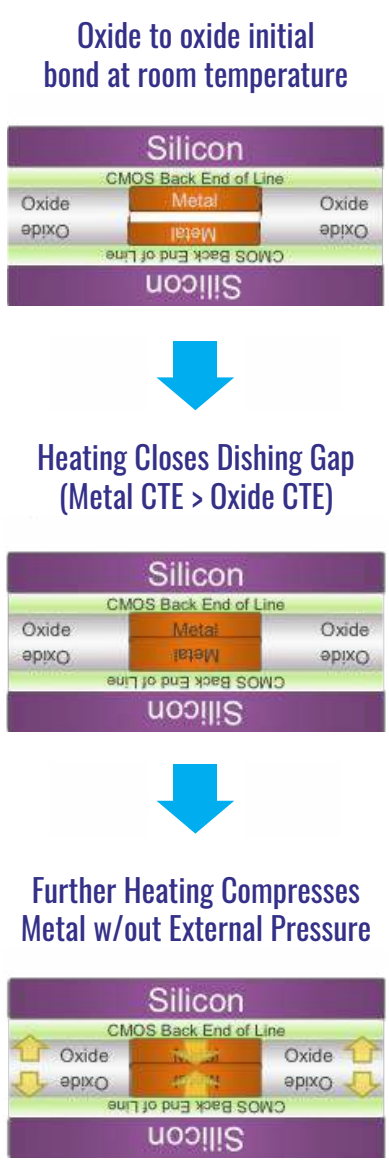

Figure 1: DBI bonding process

needed a bonding solution that would allow for fine-line lithography after bonding. The pair turned to Q.Y. Tong, described by Fountain as "the leading guru in wafer bonding", and then manager of RTI's wafer bonding lab. Together over the next few years, they developed and patented ZiBond®, an enhanced version of direct oxide bond that involves wafer-to-wafer processing at low temperatures (150-300°C) to initiate high bond strength rivaling silicon.

"What differentiates ZiBond from other direct oxide bonds? "It's not just an oxide bond," explained Fountain. "ZiBond requires the wafer or die surface preparation to be done in such a way that you reach a certain bond strength at a certain temperature." Exactly what those parameters are is part of the secret sauce. ZiBond is the dielectric bond that forms the basis for DBI.

Ziptronix and the Road to DBI

Armed with the ZiBond patent, Fountain, Enquist, Tong and several other colleagues founded Ziptronix in 2000 as a spin-out of RTI. What was Fountain's vision for the company next? To combine the dielectric bond with embedded metal to simultaneously bond wafers and form the interconnects.

He gives Enquist most of the credit. "Paul was the guy with the vision. I was just the guy in the lab turning the cranks," he says.

I compared them to Woz and Jobs. He laughs and says, "Paul is a brilliant guy with a lot of good ideas. He has a feel for what would be good for the industry."

At the time, the holy grail of 3D stacking was how to stack parts and form the interconnect as part of the bond process at finer pitches than was currently possible using wire bonding. Early prototypes involved cleaning and mounting dies on wafers using ZiBond, and then forming the top connections or through the back of wafer with "brute force" methods to connect bond pad to bond pad. Fountain noted that Sony dabbled in this staple-like approach, but the structures were big. They needed to find a more compact and efficient way to make these connections.

Fast forward to 2005 and the emergence of DBI (Figure 2). The solution was to start with an oxide bond with embedded metal recessed into it. Heat forces the metal together because it expands more than the oxide, causing it to bond, explained Fountain. Initially, nickel was the contact material used because it polished well with oxide, and some

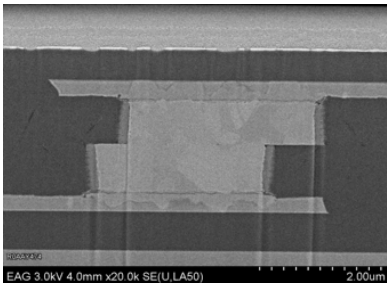

Figure 2: 10um pitch Ni DBI daisy chain connection with Aluminum routing layer (Ziptronix 2010)

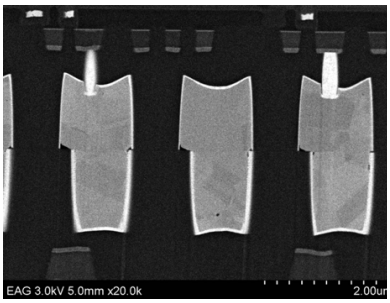

Figure 3: 2µm pitch Cu DBI wafer to wafer stack (Ziptronix 2011)

are still using it. The first applications to implement DBI were small pitch parts for focal plane arrays. They had to reach sub 10µm pitch with 3µm diameter pads.

Addressing the Challenges

As foundries don't like to work with nickel, it was important to get Cu to work with the process. The biggest challenge involved surface cleaning and achieving surface topology (Figure 3).

"Adhesives are tolerant of particles," explained Fountain. "DBI requires particle-free clean surfaces. Additionally, the surface and oxide must be smooth, and the metal has to be slightly below the surface."

The team figured a few things out along the journey, like what materials worked best for Cu and barrier polish and played around with pushing temperatures as low as possible to expand the process window to more applications, such as memory and compound semiconductors.

"We found that we could readily address engineering challenges associated with cleaning and damascene utilizing the existing equipment sets in foundries today," noted Fountain. "Damascene copper is their bread and butter. To complete the fabrication process with a surface that can be bonded seems like a natural progression."

Advantages of DBI

Fountain says DBI overcomes many of the process challenges that plague TCB, such as alignment, and bond strength at tighter pitches. The initial bond forms instantaneously, the alignment of the parts work well, and they don't slip or move as the bond is strengthened during the low-temperature annealing process. Moreover, the annealing process can be done in batches later, which speeds up the process and improves throughput.

With TCB, parts have to be held in place while heating. DBI is limited only by the alignment capabilities of the bonding tool. 1.5µm pitch is the tightest so far at the die level, but that's because the tools can't go smaller, explained Fountain. Moreover, the final bond is stronger because unlike TCB, the bond forms at both the oxide and metal interfaces, not the metal only.

Other approaches to hybrid bonding that call for adhesives or mixed metals don't form as strong a bond as a single metal, explained Fountain. Adhesives can cause reliability issues due to thermal cycling. Additionally, the bond is hermetic, which positively impacts the reliability of the end device.

DBI's Journey to Adoption

Despite its elegance, it took a while for DBI to take off. Fountain attributes that mainly to the industry's resistance to change. Early adopters had a need that wasn't being met in other ways. For example, Sony was building its image sensors with adhesives and reached distortion limits with lithography.

"We put a lot of work into this technology because we wanted to see it become a useful platform for the industry. It made sense to me that Moore's law would be expanded by going vertical. Having efficient ways to combine things would be the way of the future," noted Fountain. "We were a bit ahead of our time,

and it took a while to get traction with the technology. But now we are seeing more and more adopters in the industry."

The Journey Continues

Several licenses and an acquisition in 2015 by Tessera Technologies (now Xperi) later, Fountain and his team continue to improve DBI, not only to better understand the polishing processes but to achieve ever-changing device requirements so that it can handle a wide range of applications and pitch sizes.

Most recently, Fountain and his colleagues are working on scalable high-volume die-to-wafer bonding, working with different pitch and pad sizes to accommodate high-speed pick-and-place tools that have only 7-9µm alignment accuracy, and a double-sided die preparation process to enable sequential stacking for the memory market.

"DBI worked easily at smaller pitches and pad sizes because Cu dishing isn't an issue. With larger pad sizes it's more difficult to get appropriate dishing and a flat oxide surface," explained Fountain. "We've expanded the size of pads we can polish to 15-20µm." Metrology for surface topography check has been key to this development work, he added, crediting his atomic force microscope as the core tool for this work (Figure 4).

The Million Dollar Question

Will DBI become process of record (POR) across all 3D IC stacking approaches? Fountain is confident that it can and ticked off the reasons why: It's compatible with foundry processes, and parts can be prepared for bonding right off the line in the fab or OSAT. It can handle fine or large features (Figure 5). Its reliability is good for thermal cycling, high-temperature storage, and high humidity, which is why it's suited to automotive applications.

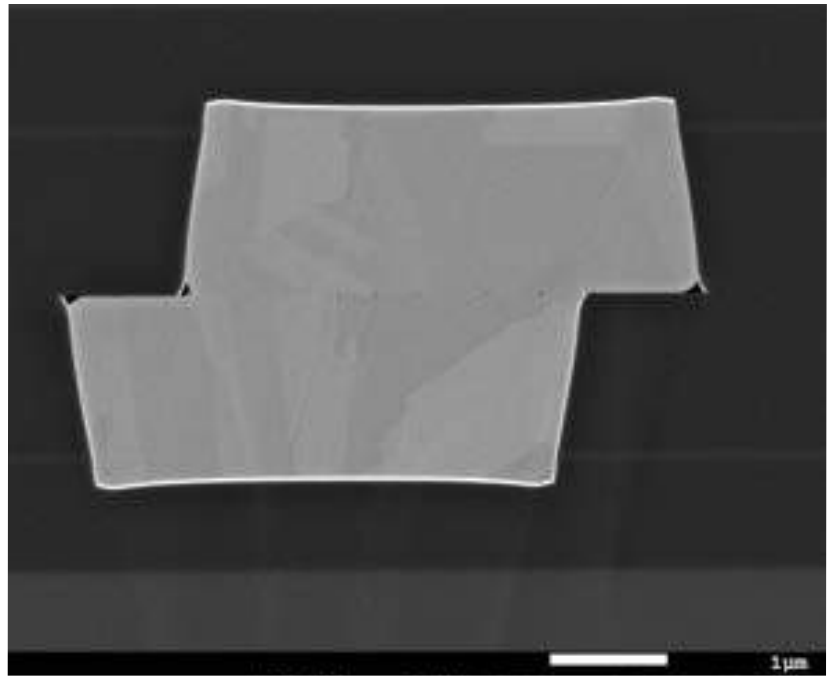

Figure 5: 10µm pitch Cu DBI after 2000 temperature cycles of -40°C to 150°C (Xperi 2018)

"It's got a lot of potential. It's what I've known and grown up with my whole career. I have a lot of confidence in it. I've seen it do amazing things and have high hopes for its use in the future," said Fountain.

"The fact that a little place in North Carolina could have come up with something that is valuable to a company like Sony just blows my mind," he added.

Yes indeed. Now I know why Gill Fountain was voted Engineer of the Year. Well done. ~ *FvT*

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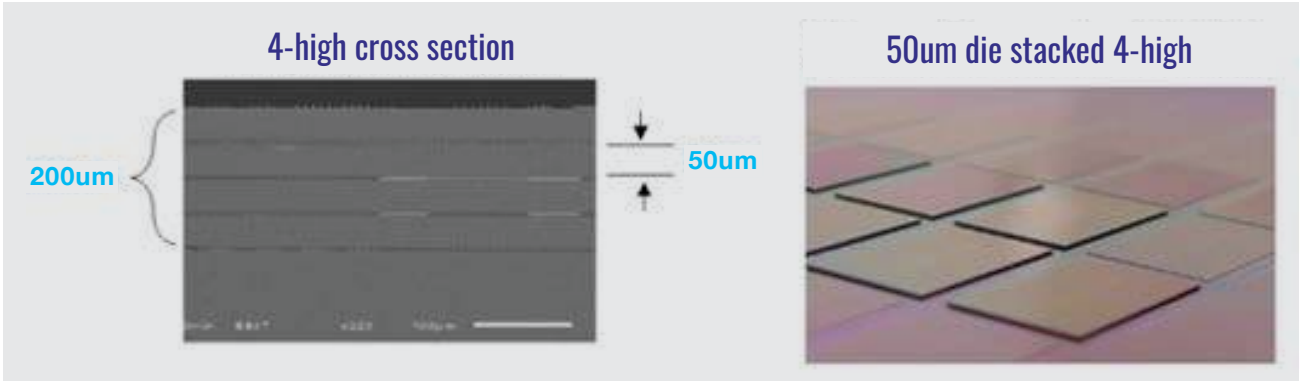

Figure 4: high DBI Die to wafer stack with 50µm thick die processed at Xperi

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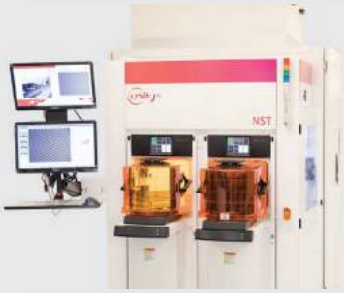

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Advanced Packaging: An IFTLE Historical Perspective

By Dr. Philip Garrou, Microelectronic Consultants of NC

On this 10th Anniversary of 3DInCites, I thought it would be a good idea for Packaging InCites from the Leading Edge (IFTLE) to look back at advanced packaging's evolution through 50 years and see how we came to be where we are.

The point of the package

From the beginning, packaging has been subservient to the integrated circuits (ICs) that they contain. As ICs became more complex, so too did the packaging and interconnect technologies that allowed the chips to be connected and create circuits to accomplish specific tasks.

The chip's package must always provide:

- Circuit protection / handling
- Form factor for testing
- Heat dissipation
- Signal and power distribution

While the dimensions on ICs have continued to shrink year over year in accordance with Moore's Law, dimensions on printed circuit boards (PCBs), where the packaged chips are interconnected, have not been able to keep pace. Thus, the package must also serve as a "space transformer" (i.e. an "interposer") to bridge the gap between the connection pads on the chip and the connection pads on the PCB, which are usually miss-matched by at least an order of magnitude.

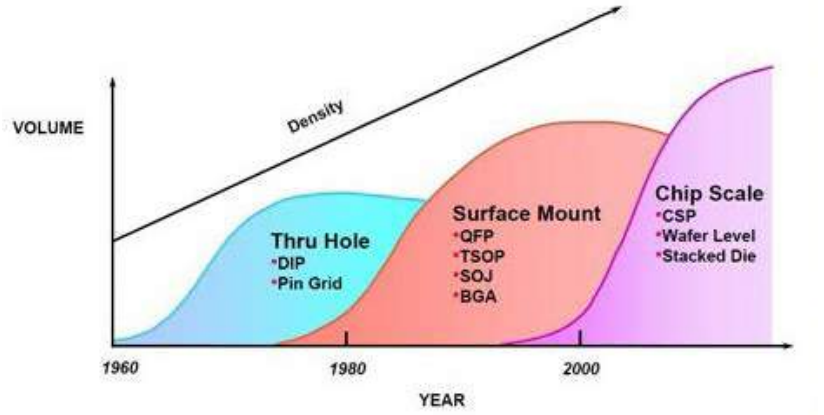


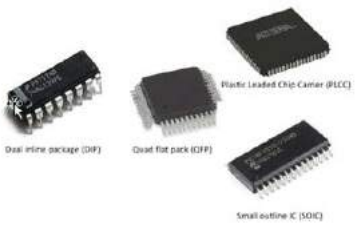
Figure 1: Packaging evolution through the decades

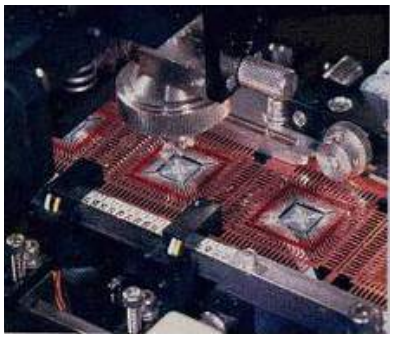
As shown in Figure 1, as we approached the 21st century, chip interconnection evolved through three distinct generations. Initially chips were mounted on lead frames and the leads inserted into holes on the PCB and soldered in place. In the surface mount technology (SMT) era in the 1980s-90s, the leads were bent into the horizontal plane, so the chips could be soldered to connection pads which were formed on the PCB, to make assembly much more cost efficient (Figure 2A-C).

From wire bond to flip chip

Packaging technology continued to evolve through the decades to meet miniaturization requirements, while at the same time offering more input/output (I/O) by moving from peripheral wire bonded (WB) technology to area array connection technology. Packages initially used WB, and thus the leads existed only on the chip's periphery. The package size was thus determined by the required number of leads and their pitch.

As ICs evolved, more I/O were required then could be accommodated on the periphery (at a usable pitch), which necessitated a change from peripheral to area array formats, affording many more I/O at the same pitch. During the SMT era, this led to the commercialization of the ball grid array (BGA) package which functioned to





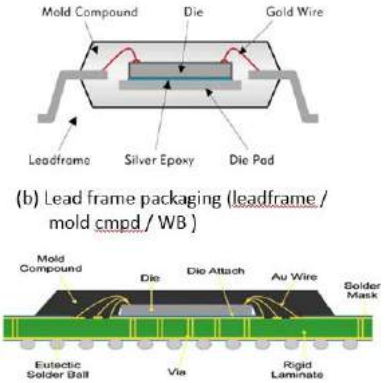


Figure 2: Peripheral Lead frame packages evolve to the BGA

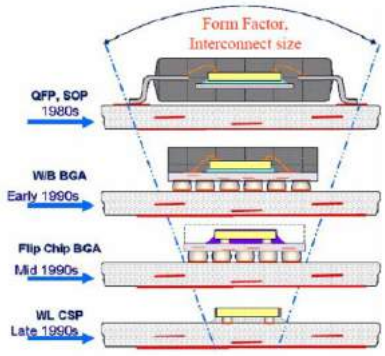


Figure 3: SMT lead frame packages evolved to the WLP.

fan out the IC pitch to an area array (Figure 2D).

Ideally, the IC package should be small and add as little additional interconnect length as possible (to minimize electrical performance degradation). Flip chip (FC) interconnect technology enabled smaller overall package sizes, an area array interconnect footprint, and improved electrical performance.

The concept of interconnecting a chip with solder bumps in an area array can be traced back to IBM's introduction of their system 360 mainframe computer in 1964. For several decades after, flip chip was confined to high-end main frame computer companies like IBM, NEC, Fujitsu, and Hitachi because it was limited to ceramic packaging due to the mismatch between the coefficient of thermal expansion (CTE) of Si and the PCB substrate [3 ppm/°C vs. 16 ppm/°C (FR4)].

In 1992, Tsukada of IBM Japan published reports that bumped chips could be reliably attached directly to printed wire board laminate if the chips were underfilled. This announcement drove the packaging community to take a hard look at flip chip technology in a broader application space. By the mid-1990s Motorola had introduced flip chip on board (FCOB) into the StarTac handset.

By the mid-1990s the miniaturization required by cell phones and other portable products created demand for a "chip scale package" (CSP) also called wafer level chip scale package (WLCSP), or more simply, the wafer-level package (WLP). In WLP technology small

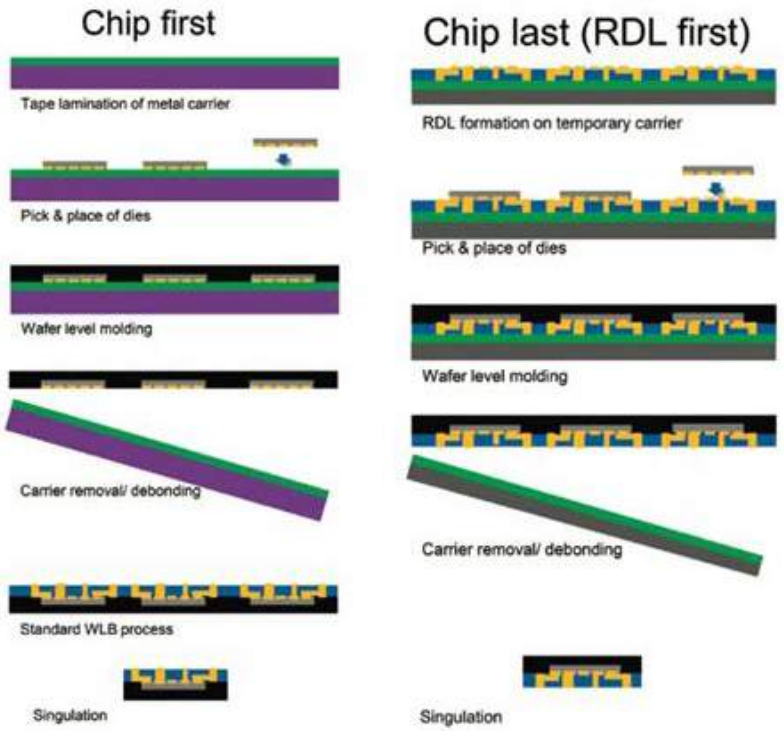


Figure 4: Chips-first and chips-last fan-out packaging

chips are bumped with the correct size and pitch bumps to allow them to be directly mounted onto PCBs without further packaging.

Since all I/O in WLCSP had to exist under the chip, the package technology soon became I/O limited. Once miniaturization reached chip size it had two options for future advancement.

For option one, the industry developed a series of packages that were called "fan-out". Fan-out WLP (FOWLP) is "re-configured" by placing known-good ICs face down on a foil and over-molding them. These molded wafers are then flipped and processed in the wafer fab with redistribution layer (RDL)/ball placement and diced. Alternatively, the interconnect is created first, and the die is connected after the interconnect is formed (Figure 4).

Packaging goes vertical

For option two, the chips are stacked and connected vertically. Figure 5 shows the first wave of vertical stacking, which used WB to stack chips on a common base. The second wave stacked package-on-package (PoP) and the 3rd wave, seeking to miniaturize as much as possible, connected die-to-die directly through thinned silicon, resulting in die-to-die interconnect lengths that could be as small as 50µm.

3DICs arrive on the scene

The 3rd wave of vertical stacking became known as 3DIC, which, by

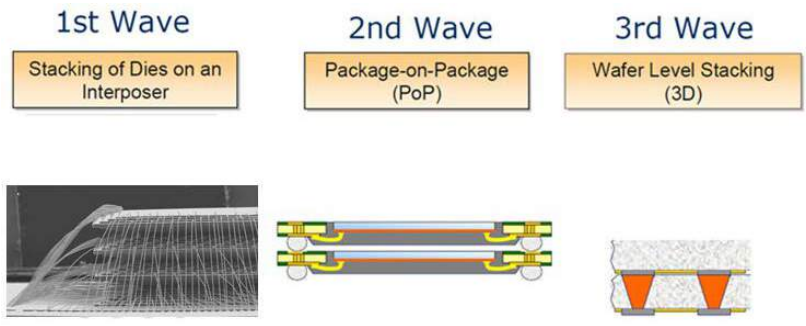


Figure 5: Chip packaging goes vertical

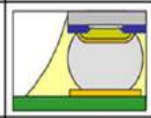
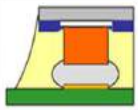
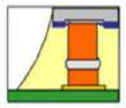
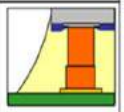
Bonding Method	C4 FC (Contolled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um

Figure 6: Miniaturization of vertical interconnect.

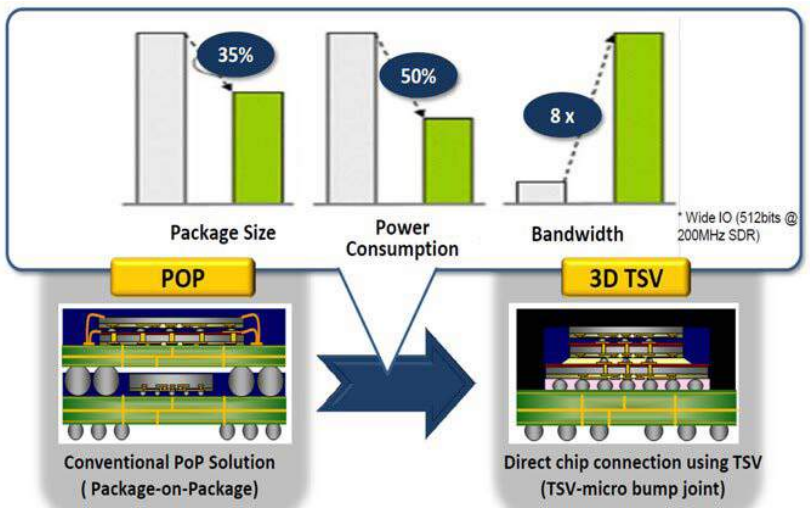


Figure 7: Samsung compares PoP to 3D with TSV.

definition, required through silicon vias (TSV), thinning down to 50µm and a die-to-die area array connection technology. As bump connection pitch gets tighter the technology required a move from tin/lead or lead-free solder bumps to so-called copper pillar bumps (CPB), where solder is placed on the tip of a plated copper pillar (Figure 6). For finer pitches, thermo-compression bonding (TCB) must replace mass reflow. At sub 30µm pitch, we will likely need a direct Cu-Cu bonding technology to avoid solder shorting and lower signal degradation.

What created high demand for 3DIC were studies, such as one done at Samsung (Figure 7) where identical systems were compared in PoP and 3DIC. The 3DIC solution showed significant size reduction, power savings and 8X increase in bandwidth.

While it was clear that 3DIC resulted in the best possible miniaturization and best possible electrical performance, it required that chip sizes match, and I/O be standardized. It was obvious that it was best suited for memory stacks where those criteria could be easily met. Hynix and Samsung introduced memory stack products in 2014-2015. High bandwidth memory (HBM) was adopted as an Industry standard by JEDEC in 2013.

While waiting for 3DIC logic, an impatient industry developed “2.5D” technology where a memory stack could be connected on a high density (<1um L/s) silicon interposer to other chip functions. The first such commercial product was developed by Xilinx and TSMC in 2011-2012 where a mega-FPGA was broken up into four segments to increase yields and then reassembled on a high-density silicon interposer.

The graphics module market has also been active in 2.5D with AMD and Nvidia introducing products in 2015-2016 and Intel introducing a high-performance compute module (HPC) in 2015 (Figure 8)

3DIC has also been active in the CMOS Image sensor (CIS) area. In 2008 Toshiba commercialized the first CIS technology using thinned die and backside TSV, but no

Figure 8: 2.5D product introductions

die-to-die stacking. By 2015 Sony announced the separation of the sensor and the circuitry and in 2017 Sony announced the industry’s first 3-Layer stacked CIS (90nm-generation backside-illuminated CIS top chip, 30nm generation DRAM middle chip, and a 40nm generation image signal processor (ISP) bottom chip).

Most technologists currently agree that 2.5D and 3DIC solutions will be key technologies for future developments in areas such as artificial Intelligence (AI), HPC and robotics, just to name a few.

The chiplet concept

A new approach to chip design is also making use of 2.5D technology. In the same way that Xilinx broke up their large FPGA into four smaller “chiplets”, which could be subsequently reconnected, large

Continued on page 60

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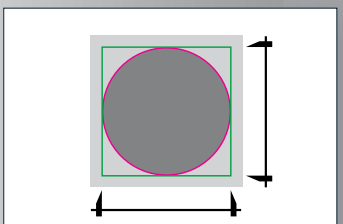
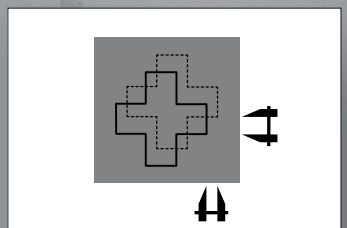
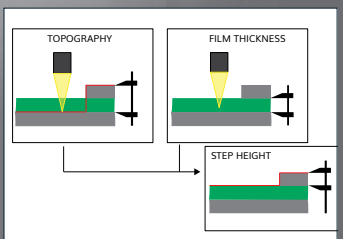


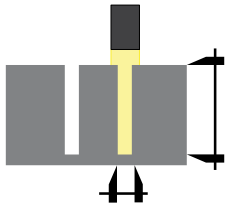
Critical dimensions



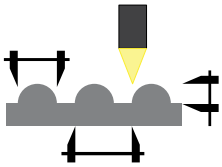
Overlay measurement



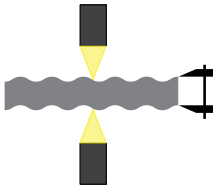
Hybrid metrology



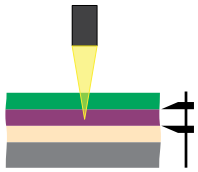
High aspect ratio vias and trenches



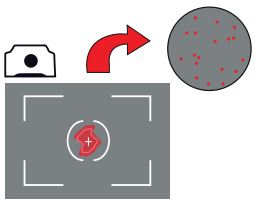
Bump dimensions and coplanarity



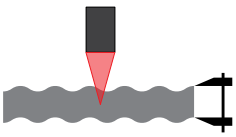
SEMI-compliant thickness and TTV measurement



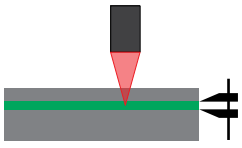
Thin film and layer stack measurement



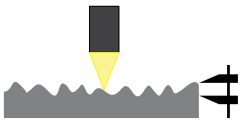
Defect inspection



Wafer and layer thickness using IR technology



Bond layer thickness using IR technology



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Why Today's Advanced Packages Need Better Inspection

By Françoise von Trapp

It's almost ironic. As CMOS scaling (aka: Moore's Law) has slowed due to the increased complexity and cost of achieving smaller nodes, the focus has shifted to advanced packaging and heterogeneous integration to meet demands for microelectronics devices targeting the internet of things (IoT) market. These devices perform a variety of functions (sensing, processing, remembering, transmitting) in smaller spaces using less power. Consequently, advanced packages are therefore designed with finer features that require higher density metal patterns, and multi-layer redistribution layers (RDLs).

And suddenly, advanced packages have become as complicated and valuable as the chips they are designed to integrate and protect. With higher value comes a higher concern for improved reliability and yields. As a result, foundries who have expanded their advanced wafer level packaging (AWLP) capabilities and outsourced assembly and test service (OSATS) providers are demanding more sensitive, inspection, metrology, and data analysis—and more accurate identification of bad parts. Not quite the level of inspection used in the front end… but something fairly close.

I interviewed KLA's Lena Nicolaides, Stephen Hiebert, and Pieter Vandewalle to learn about the company's recent developments in metrology and inspection for AWLP and final package inspection, designed to address some defect types that have become more prevalent as advanced packages have become more delicate.

The role of defect inspection

Defect challenges for WLP include smaller killer defects due to feature sizes, nuisance defects due to complex, dense metal patterns, and high warp wafers and film frame carriers for accommodating

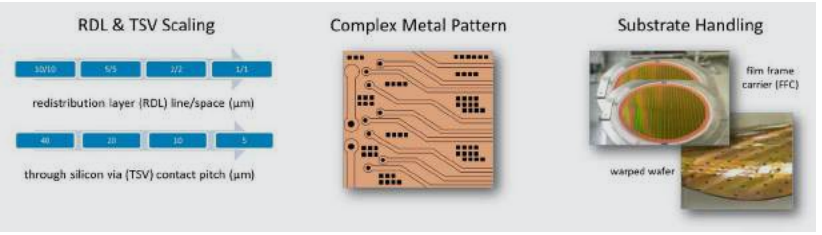


Figure 1: Defect challenges associated with advanced WLP processes, particularly fan-out-wafer-level packaging (FOWLP)

different thickness wafers, as well as reconstituted wafers (Figure 1).

As Hiebert explained it, defect inspection is particularly important during wafer level packaging processes for quality control, process control, and engineering analysis. It helps identify excursions while they can still be reworked and repaired, and again to identify defects that can't be fixed but can cause more problems if they are allowed to

approach to fan-out wafer level packaging (FOWLP), there are typically three layers of RDL and 2-5µm line/space requirements," said Hiebert. "this calls for up to 16 inline inspection steps."

These come at different points throughout the process, the most critical are after the lithography develop step, and again after the etch process in base-metal etch.

Figure 2a: KLA introduced two new inspection solutions targeting advanced WLP

continue through the processes. Through in-line monitoring, causes of defects can be characterized, and the processes tweaked, with the goal of improving final yields.

Additionally, increased package complexity calls for additional inspection steps. "In a chips-first

Defect inspection plays a similar role in test and assembly, although the focus is on outgoing quality control, and not necessarily process control. What's different for the newest wafer level packages, explained Vandewalle, is that previously wafer level packages did not go through the same test and in-

spection as legacy packages, such as lead frame and substrate-based packages. But now, high-end node chips manufactured with low-k materials, which are more brittle and subject to defects (especially after dicing), require advanced inspection, especially to capture chipping, hairline cracks, and laser groove cracks.

"One reason we decided to pursue this market was that there is no good technology outside of an R&D environment, designed to capture these types of new defects," he explained. "So, we invested in new IR-based technology for the production environment."

KLA solutions

More than three years in development, KLA recently launched two new systems, the Kronos™ 1080 and the ICOS™ F160, targeting some specific needs of advanced wafer level, 2.5D and 3D integrated packages (Figure 2).

Figure 2b

Building on lessons learned with their front-end systems, as well as their existing packaging offerings, CIRCL™-AP, and the ICOS™ line, the company worked in close partnership with its existing customers to identify the gaps in current inspection strategies, and develop these systems, explained Nicolaides

"Our customers who lead in scaling technology came to KLA looking for sensitivity beyond what the back-end players could traditionally achieve," she explained. "We designed these systems' architecture and algorithms for a superior cost of ownership, ability to find defects while offering increased throughput and overall yield improvement."

AWLP process inspection

The Kronos 1080 system is designed to inspect AWLP process steps, providing information on the full range of defect types for inline process control through multi-mode optics and sensors and advanced defect detection algorithms. Its proprietary FlexPoint™ technology focuses the inspection system on key areas within the die where defects would have the highest impact (Figure 3).

Final package Inspection

Vandewalle described the challenges in final package inspection that the ICOS F160 is designed to

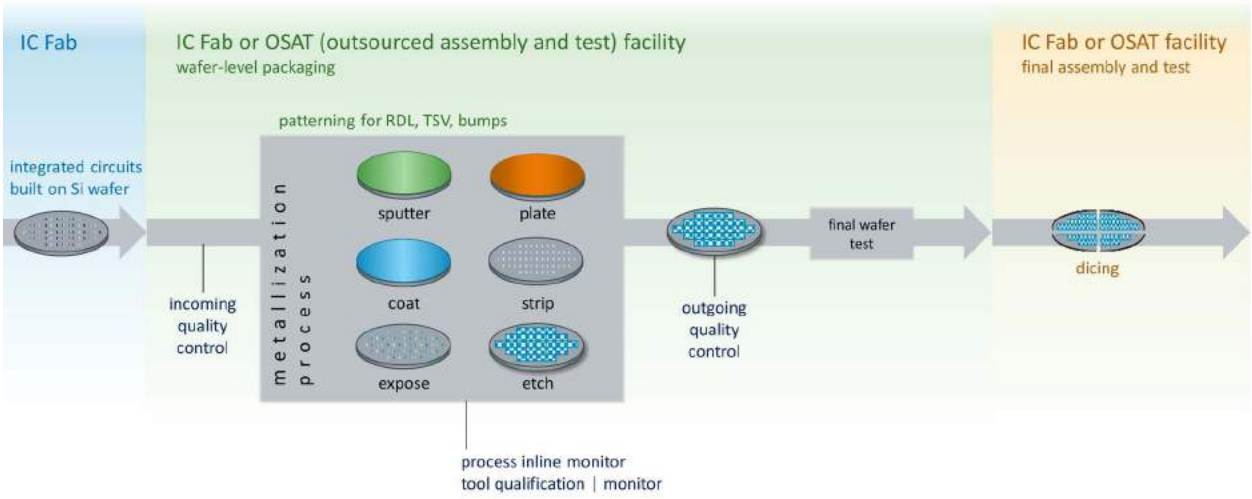


Figure 3: Kronos 1080 inspects the incoming wafers, performs in-line inspection at specific inflection points when wafers can be reworked, and then is used for outgoing quality control

address, namely low-k cracks on sidewall and laser grooves that are difficult to detect. The system's purpose is to be used in high-volume manufacturing to separate out the bad parts and keep the good.

In designing the ICOS F160, Vandewalle said the focus was finding a solution to address dicing cracks caused by an aggressive dicing practice. Existing approaches relied on either optical or open/short tests, but none was good enough to capture critical defects. He said that as a result, the packages fail in the end-use device, and mobile and wearable companies are suffering from the slip-through.

The ICOS F160 features IR inspection, which provides robust detection of invisible killer crack defects for fan-in WLP, memory and bare die. In combination with 6-side optical inspection with pre- and post-placement inspection, the ICOS F160 enables high die sorting accuracy. Additionally, the system's flexibility allows it to support a variety of workflows, including wafer-to-tape and tape-to-tape. Lastly, fast conversions, automatic calibration, and precision die pickup addresses the needs of high-volume manufacturing (Figure 4).

Figure 4: ICOS F160 key technologies to address high volume die sort challenge.

Where the action is

While CMOS scaling may continue, advanced WLP is clearly where the action is, driven by the IoT explosion. Because advanced packaging technologies are so much more varied than front-end processes, the greatest challenge for KLA was developing systems next-generation inspection systems that are both flexible and high-performing.

"There's always a trade-off. The more flexible you make something, the more challenging it is to achieve optimized performance," said Nicolaides. "After analyzing the requirements of the diverse package designs, we focused on defect sensitivity and inflection points to leverage our optical expertise."

The result of that focus has been realized in the addition of these two systems to their product portfolio. *~ FvT*

Diversification of Markets Calls for Hybrid Metrology with Multi-Sensor Technology

By Françoise von Trapp

People used to think about metrology for front-end process control and inspection in semiconductor manufacturing only. As wafer level packaging (WLP) and heterogeneous integration (HI) approaches became more advanced, metrology processes began creeping into back-end process control, where measurement becomes trickier and more diversified. I spoke with Thomas Fries, CEO of FRT, winner of the 2018 3D InCites Equipment Supplier of the Year Award. We talked about how technology diversification is here to stay, and how hybrid metrology solutions using multi-sensor technology are becoming necessary.

Figure 1: Thomas Fries, CEO FRT, accepts the 3DInCites Award outside the FRT cleanroom

Metrology for Advanced Packaging

"For the past two years, we've had a strong demand for tools that perform different metrology tasks," noted Fries. "Inspection used to be the standard, but now metrology is becoming a must-have." He went on to explain the impact the lack of mainstream processes is having on metrology solutions providers.

Despite continued efforts to scale CMOS structures to smaller nodes, metrology needs are fairly straightforward thanks to standardization of tools and processes. This is not the situation for metrology in the advanced packaging space. Measuring total thickness variation (TTV) on a wafer is not the same as measuring TTV with a very high lateral resolution. Additionally, through silicon vias (TSVs), Cu bump or pillar heights, as well as thinning, bonding and stacking are bringing new metrology needs compared to classical process steps.

Diversity changes everything

The dawn of fan-out (FO) processes both at the wafer and panel level has added more diversity to metrology needs. Add to that 2.5D and 3D heterogeneous integration, and now chiplet technologies and the diversity of the space continues to broaden. This is not the volume-driven market tier-one metrology tool providers are used to serving.

"With MicroProf® AP, we succeed to accommodate measurement requirements for different processes, and we are able to handle both wafers and panels, thinned and bonded wafers, and film frames," noted Fries.

Additionally, he says he doesn't expect the players to settle on one approach for all, because different applications call for different device architectures, which in turn require different processes. He does, however, expect a narrowing of options.

"For FRT this is a fantastic situation," said Fries. "Our early decision to focus on building tools with multiple sensors and to program our own software in-house is paying off. We are perfectly set up for doing hybrid metrology with multi-sensor technology, which is what is needed for these complex processes."

The hybrid metrology solution

So what exactly is hybrid metrology? Fries explains that for FRT, it means using its multi-sensor concept so that in one recipe, different properties on a device can be automatically measured. Up to ten fully integrated sensors act as one to automatically embed different information and create new information that isn't directly available.

Fries explained further: In the same tool, you can now, for example, measure the height of a Cu bump against the oxide in silicon in the same machine. The step height of the Cu is measured optically, and a film thickness sensor is used to measure oxide thickness. By subtraction, the film thickness, the height of the Cu above the oxide can be determined.

Additionally, with the company's third generation of tools, the up-to-date, in-house developed software, achieves 64-bit status.

MicroProf® AP

FRT recently launched a new wafer metrology tool, the MicroProf® AP, designed for advanced packaging. It allows fully automated processing of 300mm FOUPS/FOSBs and 300 mm/200 mm/150mm open cassettes. The system can handle SEMI standard wafers, highly warped wafers (e.g. eWLB), bonded wafers, wafers on tape, TAIKO, bare and thinned wafers, and even fan-out wafers. Moreover, the tool can be configured for processing frame cassettes and handling of panels. The handling part features a robot with end-effector, two load ports including mapper and RFID reader, pre-aligner and optional OCR reader stations. It can be used for all metrology tasks within the advanced packaging process, e.g. measurement of photo resist (PR) coatings and structuring, through silicon vias (TSVs) or trenches after etching, µ-bumps and Cu pillars, as well as for the measurement in thinning, bonding and stacking processes.

As standard configuration, the MicroProf® AP is equipped with a granite base setup, with a three- point sample fixture or a vacuum chuck. Besides that, numerous features can be added or retrofitted on site at a later time.

RT practices the Art of Metrology

This so-called hybrid metrology tool is the perfect fit for diversified markets, says Fries. “It paradoxically solves what the customer wants: a standard tool that can follow an established roadmap with on-site upgrades and can also handle diverse process steps and the ability to customize solutions,” he said.

Serving niche markets

Fries firmly believes that the key to success does not lie in trying to be all things to all people. With this in mind, his strategy is to focus on three growing specific markets: advanced packaging, MEMS, and LED applications.

“The market is interesting and gives us lots of options. But it’s important that we focus on niche markets and not try to do everything,” he said. “The newest, hottest applications call for new processes and metrology tools and have to be flexible to adapt to new process quickly. This isn’t what the tier-one suppliers focus on. They aren’t keen on serving niche markets because the low volumes don’t make it worthwhile.”

As a result, he says the competitive overlap is diminishing. “We don’t meet most of those competitors in the market anymore,” notes Fries. “There’s room for all of us to succeed.”

The best of both worlds

What Fries likes best about FRT is having the flexibility and capability to serve both niche and high-volume markets. The company’s hybrid metrology and inspection solutions suit the current climate of application diversity perfectly.

Usually, a company decides to pursue tier-one or niche customers. This is not the case for FRT. Even though they focus on serving the niche markets, their toolbox allows them to support both, combining the best of both worlds.

Measure the Immeasurable

By the magic of FRT’s software developed in-house, it is possible to measure things that previously couldn’t be measured. The configuration of various measurement tasks using different sensors to run consecutively within a measurement sequence is simplified. Add to that, this software provides comprehensive capabilities, from manual measurement on the device to fully automated measurement with one button operation and integration into production control systems, e.g. via a SECS/GEM interface.

By using a hybrid metrology concept - this multi-sensor metrology tool enhances the precision of measurements on samples where a single sensor or measuring principle is just not enough. Depending on the task, this may include measurements with different topography and (film) thickness sensors that are fully automated by a single recipe.

3D Test: No Longer a Bottleneck!

By Erik Jan Marinissen – imec, Leuven (Belgium)

When I joined imec in October 2008 to work on test and design-for-test (DfT) of 3D-stacked integrated circuits (ICs), there were only a few test folks active in that emerging field. Consequently, misconceptions about 3D test were omni-present. In the November 18, 2008 issue of Semiconductor International, Alexander Braun wrote: "At a symposium yesterday on 3-D integration, leading expert Philip Garrou detailed the rise of the technology as well as the challenges facing it, including test, yield, and design. (…) Test, again, will be a significant problem. Memory can be stacked as known good die, because the memory chips can be tested, but years from now, as different functions are pulled apart to stack them, there is no clear way to test them because they do not form a complete circuit. This will hold up things like the full partitioning of chips."[1] 3D InCites' tenth anniversary is a good occasion to report on the state of 3D testing and publicly declare that it's no longer a bottleneck for 3D integration.

Structural Modular Test

'Test' is an overloaded term. While some people might think of design verification (on a simulation model) or design validation (on the real chip), this article is restricted to electrical testing for manufacturing defects, typically in a high-volume setting. At this stage of product development, we assume chip designs are correct. Chip manufacturing processes are defect prone as they consist of large numbers of high-precision steps. Unavoidably things go wrong every now and then, leading to spot defects such as shorts and opens.

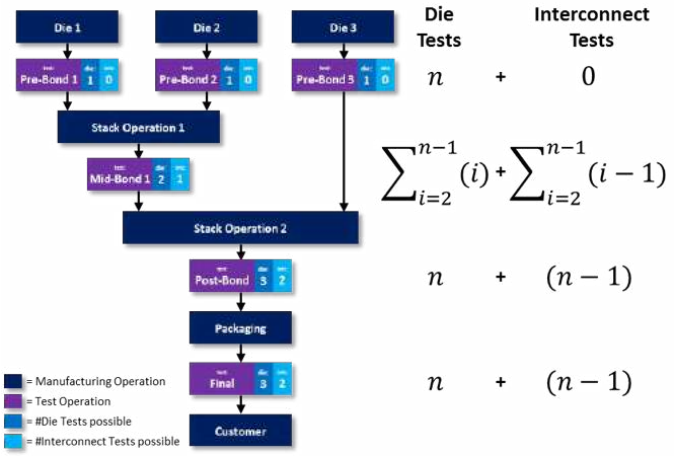
For a large chip manufactured using advanced technology, the die yield might be 80%, while customers typically tolerate defective chips in quantities of no more than 100 defective parts per million (dppm). Consequently, a test needs to be a very effective filter for defective chips. Because every transistor or interconnect segment on a chip can suffer from defects, each chip needs to be tested, and hence the test needs to be very efficient; taking no more than a few seconds per chip in a fully automated process.

During test, stimuli are fed into the chip and corresponding responses on the chip outputs are compared to expected responses to determine 'pass' or 'fail'. Automatic test pattern generation (ATPG) tools, available from all major EDA suppliers, try to cover as many potential fault locations as possible with a minimum of test patterns to reduce test time and associated cost.

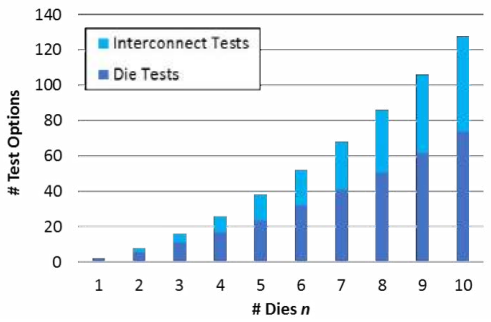
ATPG tools do not utilize application knowledge of the device-under-test (DUT), but instead base themselves on the DUT's structure: the gate-level netlist with interconnected library-cell instances (AND, OR, flip-flop, etc.). The resulting test patterns have no relation with the mission-mode ('functional') operation of the chip, but check if these cells are present, operational, and correctly interconnected. We refer to this as a structural test (as opposed to a functional test).

For a structural test, testing a single die that only implements a partial function of a multi-die stack is no problem at all. This modular approach to test development and execution has become common practice in the industry.

Today's core-based system-on-chips (SOCs) are routinely tested in a modular fashion: core-by-core, sequentially, or at the same time.[2] For 3D integrated circuits (3D ICs), for which the various stacked dies might be designed and/or manufactured by different parties, modular testing (here: die-by-die) makes even more sense. The benefits include:



	Die Tests		Interconnect Tests
$t(n)$	n	+	0
	$\sum_{i=2}^{n-1}(i)+\sum_{i=2}^{n-1}(i-1)$		
$t(n)$	n	+	$(n-1)$
$t(n)$	n	+	$(n-1)$



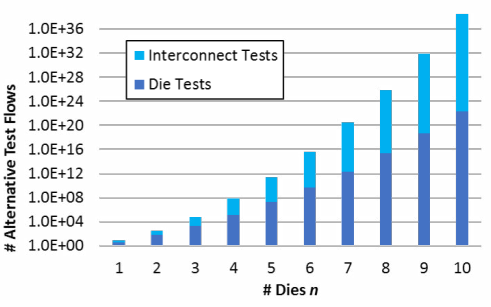


Figure 1a: Example test flow for $n=3$: maximal 11 die tests and 5 interconnect tests. Figure 1b: Equations for $t(n)$ as function of the number of dies in the stack n. Figure 1c: Number of test $t(n)$, for increasing number of stacked dies n. Figure 1d: Number of alternative test flows $f(n)$, for increasing number of stacked dies n.

- Targeted test pattern generation, tailored to the circuit type (e.g., logic or memory) and function, preferably by the team also responsible for the design
- Freedom to (re-)schedule the various die tests if manufacturing yields so require (test engineers like to put tests that are more likely to fail early in their test suite, to reduce the per-die average test time by applying 'abort-on-fail')
- Re-use of tests in case design modules are reused
- First-order fault diagnosis and yield attribution (because: if the test for a particular module fails, that module most likely contains the root cause)

Test Flow Optimization

A major difference between testing 2D and 3D ICs is the potential complexity of the test flow. At which moments in the manufacturing flow do we execute a test for what stack component? Conventional 2D chips typically have two test moments: first while still in their wafer (wafer test, a.k.a. e-sort), to avoid package costs for defective dies, and then again after assembly and packaging (final test), to guarantee the outgoing product quality toward the customer. 3D ICs have many more test moments, tests, and hence test flows. For an n-die stack, we have prior to stack assembly n possible test moments during which we can execute a pre-bond test on a die. After every stack assembly operation, we have a new test moment, in which each die and interconnect layer in the stack built up so far can be tested. We refer to these test moments as mid-bond tests (for partial stacks) and post-bond tests (for complete stacks). There are $\sum_{i=2}^{n} (i)$ die tests and $\sum_{i=2}^{n} (i-1)$ interconnect tests possible during these test moments. After packaging, the final test can contain n-die tests and $(n-1)$ interconnect tests. In total, an n-die stack has $2n$ test moments during which a grand total of $2n-1+\sum_{i=2}^{n}(i)$ die tests and $n-1+\sum_{i=2}^{n}(i-1)$ interconnect tests might occur. In practice, there might be no physical test access during certain test moments, which reduces the number of feasible tests. A test flow consists of an execution decision (yes/no) for each test at each feasible test moment. If a die stack has a total of $t(n)$ tests, this allows for $f(n)= 2^{t(n)}$ alternative test flows. Note: this definition of $f(n)$ does not account for alternative test schedules due to reordering of tests at a particular test moment.

Figure 1(a) illustrates the test flows for a relatively simple stack with only three dies, resulting in 16 tests (11 die + 5 interconnect tests), and therefore a total of 216 = 65,536 alternative test flows.

In practice, some test moments might not permit probe access, and this reduces the number of feasible tests and test flows. For example, for imec's FC-FOWLP test chip consisting of seven dies, from the theoretical 68 tests only 33 tests are practically feasible; which still implies a whopping $233 \approx 8.6 \times 109$ alternative test flows.

Figure 1(b) shows the generic equations for t(n) as function of the number of stacked dies n. Figures 1(c) and 1(d) depict t(n) respectively f(n) as function of the number n of stacked dies.[3]

The large numbers of alternative test flows necessitate computer support. The 3D-COSTAR software tool, developed by TU Delft and imec, makes a cost analysis of a user-specified manufacturing and test flow.[4] The tool considers costs proper to design, as well as five manufacturing operations:

1. Wafer processing
2. Stack assembly
3. Test
4. Packaging
5. Logistics

These operations are considered not perfect and are modeled with an associated yield in percent. For test, 'yield' is defined as 100% minus the test escape rate (in dppm). 3D-COSTAR calculates the lump-sum costs per operation, where all costs are attributed to those stacks that pass the entire flow and are shipped to the customer. The tool can analyze the effect of varying

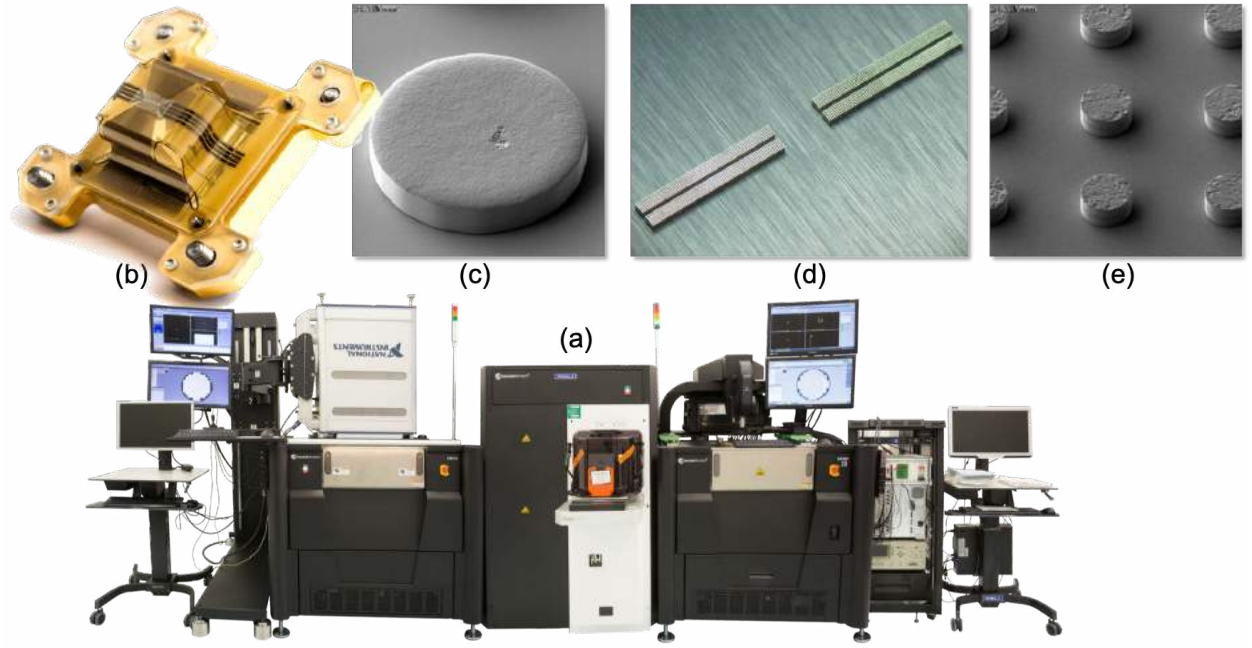


Figure 2: 'Vortex-2' test system in imec's Fab-2, based on FormFactor's CM300 probe station (a), has been used for probing large-array 40µm-pitch µbumps with advanced probe cards. FormFactor's Pyramid® RBI probe cards (b) left small probe marks on ø25µm Cu µbumps (c), and Technoprobe's TPEG™ T40 probe cards (d) left barely visible probe marks on ø15µm Cu/Ni/Sn µbumps (e).

an arbitrary number of parameters (in lock-step) along one or two independent axes, as variations of a user-defined base case. The output of the analyses is an estimation of product quality (defective chips that nevertheless pass the test, in dppm) and the cost per shipped stack, sub-divided over the subsequent manufacturing operations.

Test Access

The main challenges of 3D testing are related to test access: delivering test stimuli to where they can detect the presence of a defect, and the test responses in the opposite direction. Test access comprises two components: external test access, i.e., from the test equipment to the chip I/Os and back, and internal test access, i.e., from the chip inputs to the actual on-die defect location and back to the chip outputs.

With external test access, several challenges and their solutions related to probing on 'naked' (= not-yet-packaged) dies or die stacks are described below. Internal test access is handled by on-chip DfT hardware. The conventional ('2D') DfT has been extended with 3D-specific features, and those are described at the end of this article.

Probing Challenges and Solutions

For most product scenarios, realistic yields require a combination of pre-bond, mid-bond, and post-bond testing. This prevents manufacturing defects from being discovered too late in the stack-assembly flow thus requiring the entire stack to be scrapped, including perhaps other (defect-free) dies. Whereas test access contact for final test is made through a test socket, the pre-, mid-, and post-bond tests all depend on probe technology. For multi-die stacks, the following probing challenges have been identified and resolved in collaboration with our partners.[5]

Probing on large tape frames.
Stack-assembly flows for multi-die stacks frequently use tape frames as a temporary carrier: for diced wafers, for aggressively thinned-down wafers, for pick-n-placed dies and die stacks, etc.[6] Out of necessity, a tape frame is larger than the wafer it holds; for a ø300mm wafer, the outer dimension of the frame is ø400mm.[7]

Imec worked with Cascade Microtech (now FormFactor) to specify and implement adaptations to the CM300 probe station, so that ø300mm wafers on a large tape frame can be loaded manually.[6] The Tokyo Electron WDF™-12DP probe stations even have an automatic loader for such large tape frames.[8]

Probing ultra-thin wafers on a flexible tape.
Wafer thinning is commonly performed on dies used in multi-die stacks: from 780µm down to ~200µm to fit the stacked dies into a standard-height package cavity or, when TSVs are employed, even thinner to expose the TSVs at the wafer back-side (at imec: 50µm). Stretched UV-curable dicing tape, laminated over a tape frame, is commonly used as a temporary carrier to prevent ultra-thin wafers from sagging and curling.

The forces exercised by probe needles should be sufficiently high to guarantee an acceptable low contact resistance between each probe tip and its corresponding probe pad. However, when we do this on an ultra-thin and flexible wafer atop flexible dicing tape, we should avoid probe forces that cause permanent or even temporary stress-induced electrical or mechanical effects and damage.

At imec, we have done numerous experiments with probe cards that require different probe forces: conventional cantilever, FormFactor's

Pyramid® and Pyramid® RBI (Rocking Beam Interposer) MEMS-type probe cards, and Technoprobe's ARIANNE™ and TPEG™ probe cards. We recommend a low-force probe card in this situation.

Probing large arrays of fine-pitch micro-bumps.
The interconnect between stacked dies consists of large arrays (>1,000) of Cu and Sn micro-bumps at ultra-fine pitch: 40µm. Imec has developed a unique test system to characterize probe cards that claim to be capable of probing such micro-bump arrays. It consists of a FormFactor CM300 probe station with hard-docking National Instruments test head with 1,216 parametric tester channels.[9]

Imec has in-house manufactured test wafers with only micro-bumps (>10 million micro-bumps at 40µm pitch on a ø300mm wafer) in various metallurgies. This set-up has been successfully used to characterize advanced micro-bump probe cards which imec co-developed with leading suppliers: FormFactor's Pyramid® RBI and Technoprobe's TPEG™ T40.[10, 11]

Probing singulated dies and die stacks on a flexible tape.
The challenge is that the probe targets might have translated or rotated from their original wafer-map position, such that blind index stepping by the probe station is no longer possible. This happens when probing on diced wafers or diced stacks on dicing tape, due to the flex-n-stretch forces of the dicing tape).

Another application is pick-and-place of die-to-die stacks on a carrier substrate, as the pick-and-place tool might be insufficiently accurate for subsequent probing.[8] Together with our partner FormFactor, we have developed and successfully demonstrated software that determines the individual misalignment per die or die stack at the start of the wafer probe session and then compensates for it while probing.[8]

Originally deemed impossible when we started to work on this topic in 2011, today imec is probing 40µm-pitch micro-bump arrays on a routine basis. Recently, we reported on a case study where all probing challenges described above and their proposed solutions, were applied in a combined fashion.[5]

3D-Design-for-Test Architecture

For transportation of stimuli and responses within the die (stack), we need on-chip DfT. Conventional 2D-DfT includes internal scan chains, test data compression to handle large dies, core-test wrappers around embedded cores and other design units that will be tested as stand-alone units, and built-in self-test hardware for embedded memories. The term '3D-DfT' refers to on-chip DfT features that are explicitly added to handle 3D ICs.

A 3D-DfT architecture should support a per-die modular test approach and therefore requires wrappers at die level, such that the various dies and their inter-die interconnects can be tested independently from each other. Whereas conventional 2D core wrappers (as specified by IEEE Std 1500[12]) have one test input and one test output port, a 3D-DfT die wrapper should support multiple test ports.

A die has its test data to and from the test equipment enter and exit via its primary test port. In case one or multiple other dies are stacked directly on this die, it will also have a corresponding number of secondary test ports, which each serve as a plug for the primary test ports of one of these stacked dies. In this way, test stimuli can enter the stack through the primary test port of the base die, be transported up in the stack, possibly through other dies, to reach the destination die where they execute their defect detection work; likewise, test responses need to be transported from the DUT through other dies in the stack down to the external stack I/Os.

Imec defined and patented a 3D-DfT architecture that meets these requirements, initially for single-tower logic-on-logic die stacks (Figure 3). With Cadence Design Systems we developed EDA tool flows for DfT insertion and test generation; and we designed, manufactured (partly at GlobalFoundries, partly at imec), and tested successfully a demonstrator IC containing the proposed 3D-DfT.[13, 14]

The EDA tool flows were made available as a rapid adoption kit (RAK) to Cadence customers, used for several TSMC test chips, and released as TSMC Reference Flow for CoWoS and 3D-IC. We extended the basic architecture with provisions for memory-on-logic stacks; logic dies to be complex SOCs with a hierarchical design and test approach, containing embedded IP cores and test data compression; for multi-tower stacks to support at-speed test of the inter-die interconnects; and to create realistic test conditions by controlling the switching activity of dies and cores neighboring to the current module-under-test.[15, 16, 17, 18]

3D-DfT Standardized: IEEE Std P1838

To guarantee interoperability of the 3D-DfT architecture across the various dies in a stack, especially if these dies are designed by different teams or companies, a standardization effort was needed. This was done under the umbrella of IEEE Standards Association, as other DfT standards reside there as well.

In 2011, I founded a standardization working group under IEEE sequence number P1838. Standardization is intrinsically a slow process, but after eight years, the draft standard is finally nearing completion. At the end of 2018, the ballot group has been formed and in 2019 the actual ballot will take place, hopefully leading to an approved standard still in the same year. IEEE Std P1838 standardizes per-die 3D-DfT features, such that if compliant dies are brought together in a die stack, a basic minimum of cooperative test access is guaranteed to work across the stack.[19]

IEEE Std P1838 consists of three main components: a die wrapper register (DWR), a serial control mechanism (SCM), and a flexible parallel port (FPP). DWR and SCM are 3D extensions of existing standards IEEE Std 1500 and IEEE Std 1149.1, respectively. The FPP, a novel feature of P1838, is an optional, scalable multi-bit ('parallel')

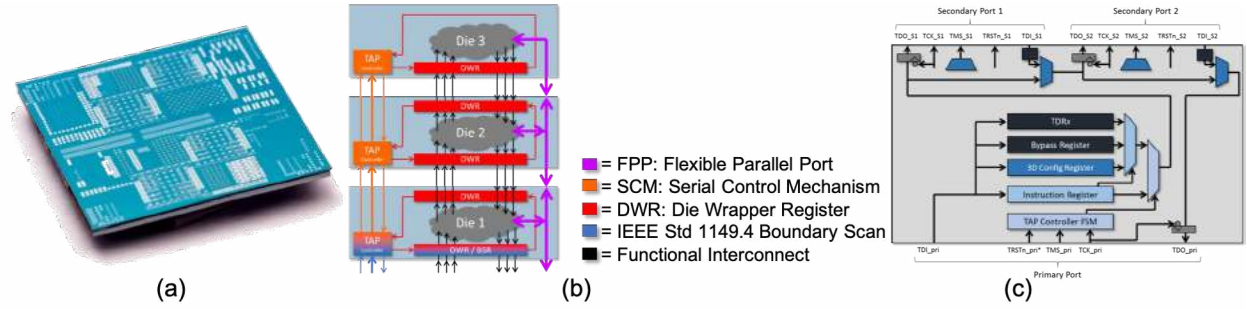


Figure 3: 'Vesuvius-3D' two-die stack containing a 3D-DfT demonstrator[14] (a), overview of the IEEE Std P1838 3D-DfT architecture (b), and detail view of P1838's serial control mechanism on a single die with two secondary ports (c)[19].

test access mechanism that offers higher bandwidth compared to the one-bit ('serial') mandatory part of P1838.[20]

Conclusion

DfT and test engineers know the limits of their work. Our industry is not making chips because the test community has developed a fancy test solution for them; customers would not care. They are interested in more performance, more storage capacity, and higher bandwidth, benefits which can be achieved with 3D ICs. But, on the other hand, our industry cannot put high volumes of products with wonderful new performance/storage/bandwidth features on the market, if these products are not individually tested for defects. Customers do not accept that.

The mere fact that the test community started working on 3D ICs was a clear sign that release of actual 3D products was imminent. With the solutions described in this article, most of the test challenges related to 3D ICs have been addressed, such that we can conclude that 'test' is no longer a bottleneck for market introduction of 3D ICs. The test community has delivered, adequately and, while the first products are hitting the market, just on time!

If you want to read more about 3D (test) challenges and solutions: they are described in detail in the book "Design, Test, and Thermal Management", edited by Paul D. Franzon (NCSU), Erik Jan Marinissen (imec), and Muhannad S. Bakir (Georgia Institute of Technology).

This book is Volume 4 in the well-known book series "Handbook of 3D Integration", published by Wiley-VCH and available from March 2019 onward.

About the Author

Erik Jan Marinissen is principal scientist at imec in Leuven, Belgium, the world-leading independent R&D center in nanoelectronics technology. His research on IC test and design-for-test covers topics as diverse as 3D-stacked ICs, CMOS below 10nm, silicon photonics, and STT-MRAMs. Marinissen is also visiting researcher at Eindhoven University of Technology in the Netherlands. Previously, Marinissen worked at NXP Semiconductors and Philips Research in Eindhoven, Nijmegen, and Sunnyvale.

Marinissen is (co-)author of 250+ journal and conference papers (h-index: 43) and (co-)inventor of 18 patent families. He has received numerous awards for his work and is very involved in IEEE conferences and standards. Among them, he served as editor-in-chief of IEEE Std 1500 and as founder/chair (currently vice-chair) of the IEEE Std P1838 Working Group on 3D-SIC test access.

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Awards Related to This Work

Erik Jan Marinissen received the Meritorious Service Award from the Test Technology Technical Council of IEEE Computer Society "for significant services as Program Chair of the IEEE International Workshop on Testing Three-Dimensional Stacked ICs (3D-TEST) since 2010".

Mottaqiallah Taouil, Said Hamdioui, and Erik Jan Marinissen received the Technology Transfer Award 2015 from HiPEAC for the 3D-COSTAR Test Flow Optimization Tool (https://www.hipeac.net/news/6774/hipeac-tech-transfer-award-2015-winners-announced/).

Imec received the Research Institute of the Year 2017 award from 3DInCites (https://www.3dincites.com/3d-incites-awards/2017-3d-incites-awards-winners/).

Ferenc Fodor, Bart De Wachter, Erik Jan Marinissen, Jörg Kiesewetter, and Ken Smith received the Engineering Impact Award 2017 from National Instruments in the category Electronics and Semiconductors for large-array fine-pitch micro-bump probing (https://forums.ni.com/t5/NI-Blog/Changing-the-World-with-Science-and-Engineering-2017-Engineering/ba-p/3615313).

Erik Jan Marinissen received the Emerging Technology Award 2017 from the IEEE Standards Association "for his passion and initiative supporting the creation of a 3D Test Standard" (https://standards.ieee.org/about/awards/etech).

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Special Section:

The Past, Present and Future of 3D Integration

On this, the occasion of the 10th Anniversary of 3D InCites, we asked our advisory board and other members of the industry to reflect on the past 10 years of the 3D integration journey, and answer two questions:

1 **What was the single most pivotal event (good or bad) in the last 10 years that impacted the commercialization of 3D integration technologies?**

2 **Looking into your crystal ball, where will 3D and heterogeneous integration technologies take us in the next 10 years?**

The responses we received ranged from insightful comments and personal reflections, to longer editorial contributions and analyses, both market and technical. Every contribution offered insight and perspective, so we chose to create this special section featuring them all. Enjoy!

3D InCites Turns 10: A Brief Analysis of the 3D Journey

By Yann Guillou, Trymax

I cannot believe 3D InCites is already turning 10! As wise people say, time flies! Taking a step back, I have to admit a lot of progress has been made since my first attendance as a young engineer to the EMC 3D workshops back in 2008. At that time, we were discussing how to form a via, how to fill it, how to use a temporary wafer carrier to process thin wafers…etc.

We are definitely more mature now (not old!) and I'm convinced 3D InCites contributed to the progress by sharing knowledge across the industry.

I'm honored to have been part of their advisory board since 2010 under the enthusiastic leadership of Françoise. Following is my simple analysis of our 3D journey so far.

The Birth of 3D

This may not be considered '3D integration' by many people (including me) but the CMOS image sensors (CIS) that use via-last through silicon via (TSV) interconnect technology were a very significant step in the commercialization of 3D. The Industry started to discover layers could be stack on top of each other with direct connections, and with much higher performances than die stack using wire bonds. This was the starting point.

The teenage years

Stacking memory dies and application process engines in high-end cell phones (now known as smartphones) was identified as

a potential killer application to deliver high bandwidth at lower power consumption and with very small vertical dimension. However, thermal budget constraints and business model/supply chain limitations killed the high hopes. Hopefully, Xilinx and AMD made them in a slightly different way. However, the volume they manufactured cannot be compared to how things would have been if a flagship smartphone manufacturer had decided to embark on using wide IO memory with processor. In the meantime, cell phones started using TSMC's integrated fan-out (InFO) in a package-on-package (PoP) configuration, which was already a great achievement with significant benefits.

Endless opportunities

I still believe that system-on-chip (SoC) disintegration with IP blocks designed at their optimized technology nodes and then stacked on top of each other could happen. This is the next step after the new system-in-package (SiP) development we see now, and it should be part of the heterogeneous integration roadmap. The recent announcement of Intel's Foveros in December 2018 confirms this is likely happening.

Let's see what 2019 brings to us!

3D Powered: From Image Sensors to Edge Computing

By Paul Werbaneth, Nor-Cal Products, Inc.

The widespread deployment of 3D stacked CMOS Image Sensors (CIS) in consumer electronics, namely smartphones, by handset makers domestic (Apple, iPhone) and overseas (Samsung, Galaxy), is certain proof that 3D integration technologies pivoted over the last ten years from being something useful only for fairly esoteric applications and high ASP products, to being a technology that reached the right market, at the right cost, at the right time, in volumes high enough to push yields up, costs down, and, in Sony's case particularly, put money in the bank.

An exploding market

According to Yole Developpement, as reported by Peter Clarke, "The (CIS) market was up 19.8% from $11.6B in 2016 mainly driven by smartphones and the desire to add improved cameras. However, Yole believes the CMOS image sensor has a bright future driven by new applications in autonomous vehicles and industrial and machine vision. By 2023 Yole predicts the annual market will have climbed to more than $23B, a compound annual growth rate of 9.4% from 2017 to 2023." That's a lot of Simoleans. And that's a lot of CIS.

As Coventor reports, "A 3D-stacked image sensor consists of a back-side illuminated (BSI) image-sensor die, face-to-face stacked on a logic die. The motivation to invest in stacked chip BSI CIS development has been varied depending upon the manufacturer but can be summarized as: 1) adding functionality; 2) decreasing form factor; 3) enabling flexible manufacturing options; and 4) facilitating optimization for each die in a 3D stack."

Who talks on their phone anymore?

Sure, people like their smartphones for texting, talking, and surfing the internet, but people really like their smartphones for recording videos and snapping still photos, and when you build a better camera into a phone you've built a better phone. Engadget UK ranks the most important smartphone features this way:

1. Design and build quality
2. Screen
3. Great camera
4. Headphone jack
5. Battery life
6. Processor power
7. Price

A picture's worth a thousand words, and even if Andy Instagram or Sally SnapChat don't know it, 3D stacked CIS have made their social media feeds insanely great.

Is AI the next stop for 3D ICs?

Where will 3D and heterogeneous integration technologies go in the next 10 years? How about leaping from big silicon in data centers to porting small silicon for on-the-fly decisions at the edge?

We already know about high-bandwidth memory (HBM) integrated with graphics processor units (GPUs) for high-performance computing applications, and in autonomous vehicles, but if the direction IBM is heading pans out, analog artificial intelligence (AI) chips using 8-bit precision in-memory multiplication with projected phase-change memory may be supplanting trillion transistor GPUs in going from "narrow AI" (puppy or muffin?) to "broader AI" (reading medical images, for example).

Since "existing hardware can't efficiently handle the largest neural networks that researchers have built," we're probably going to be heterogeneously packaging more devices, together with memory, running those 8-bit precision calculations, and deploying heterogeneously integrated SiP everywhere we need ubiquitous intelligence in the world.

3D Integration's Thousand Mile Journey

By Amy Leong, FormFactor

When we look back at the last 10 years, it's really been a series of baby steps to move the commercialization of 3D integration technologies forward. There is no single pivotal event that catalyzed the 3D evolution. Like the Chinese philosopher Lao Tzu said, "do the difficult things while they are easy and do the great things while they are small. A journey of a thousand miles begins with a single step."

Our challenging journey of 3D integration has been marked by many incremental accom

plishments and milestones. A few noteworthy events include the first commercialization of 2.5D FPGA integration by Xilinx and TSMC in 2011, mass production of high bandwidth memory (HBM) in 3D stacks by AMD and Hynix in 2015, and the latest Intel announcement of Foveros 3D chip stacking technologies in 2018. One common driver behind these innovations is to leverage advanced packaging technologies to supplement the slowing of Moore's law for transistor scaling.

From a probing technology perspective, the adoption of advanced packaging (copper (Cu) pillar, TSV, etc.) has driven rapid pitch reduction and a corresponding density increase for probe cards. Over the last 10 years, the minimum grid-array probe pitch has reduced from 150µm to 40µm, while the total probes per card has increased from ~10K probes to over 100K probes. These trends have breached some interesting thresholds:

- The diameter of a probe becomes smaller than a human hair ~100µm, it is at or beyond the positioning accuracy of most human hands.
- The manual probe assembly (~1 min. per probe) will result in longer probe card assembly time than wafer fab cycle-time of ~45 days (65k mins).

In 2013, FormFactor was the industry's first test provider to bring the automated vertical MEMS probe assembly capability to build fine-pitch, multi-site probe cards (MF100_Probes_RTsm.jpg). Today, we continue investing significantly in MEMS probe and automation capabilities, and routinely build probe cards with probes as small as 20µm, ~1/5 of a human-hair diameter. Our MEMS probe engineers humorously said, "our job is to split a hair daily!"

While the technical solutions for 3D and heterogeneous integration have been demonstrated, the commercial bottleneck remains. Today, the adoption of 3D integration is still limited to a few performance-hungry applications such as data center and artificial intelligence (AI), not widely used for consumer-driven mobile applications.

In the next 10 years, we need to drive a higher level of back-end manufacturing automation to reduce the total cost of the 3D stack. For example, many improvement opportunities exist in the areas of singulated die handling, testing, transporting, as well as process control software and data analytics, to advance the yield of the singulated thin-die and the ultimate stack.

My crystal ball sees a fully-automated and high-throughput die assembly and test floor at OSATs and foundries in the next 10 years, gradually moving away from wafer-based processing as the adoption of heterogeneous integrations increases.

3D Enables More than Moore

By Paul Lindner, Executive Technology Director, EV Group

Looking back at the last 10 years, it is very difficult to choose one single

event that was the most pivotal for commercializing 3D integration technology. There have been many prior events that have driven 3D integration and aligned the whole industry in migrating from monolithic 2D to heterogeneous and 3D integration.

From my perspective, the most path-breaking event was the rise of the backside illuminated CMOS image sensor (BSI CIS) into consumer devices about 10 years ago. To our knowledge, this was the first 3D integrated high-volume device.

But why has BSI CIS been so successful on the market, while other devices have also demonstrated performance improvements utilizing 3D integration? In my opinion, BSI CIS represents the first time that the sweet spot of performance, cost and form-factor were met in 3D integration. Without 3D integration, pixel scaling as low as 1µm today, with superior sensitivity and speed, would not have been feasible.

Processing BSI CIS also triggered the adoption of fusion bonding in high-volume manufacturing, as well as enabled hybrid bonding, which will both be fundamental building blocks for future 3D system on chip (3D SoC) as well as 3D IC with sequential processing, including layer transfer or backside power distribution.

I think we are just beginning to experience the acceleration of 3D and heterogeneous integration in a lot of different applications and markets. Where individual devices have been adapted to 3D integration with a lot of effort and engineering power in the past, 3D is imperative in the next 10 years. With both "More than Moore" and "More Moore" having a clear roadmap toward 3D integration, design kits and design tools are under development right now and will be rolled out shortly. Flexibility will be key for a fast-paced industry with shorter and shorter consumer product lifecycles. Furthermore, 3D will enable players that have dropped out of the scaling race to come back and enable high-performance devices on larger nodes at lower cost. The next 10 years will change the way we design and build systems, using 3D in significantly more applications than was the case during the past 10 years.

A Shift in Value from Single to Multi-die ICs

By Herb Reiter, eda2asic

The single most pivotal event to impact the commercialization of 3D technologies was TSMC's introduction and volume manufacturing of its integrated fan-out (InFO) packaging technology. This event demonstrated that multi-die integration can be cost-effective for high-volume applications.

Since its deployment in 2015, every new generation of iPhones has used this technology and the several hundred billion iPhones shipped have proven it to be reliable.

Based on many years of contributing to the roll-out of ASIC technology and process design kits (PDKS), as well as reference flows for enabling the transition to the fabless and foundry business model, I expect that the value-shift from single-die ICs to multi-die advanced IC packaging technologies will continue and bear fruits in these major application areas:

- Smart IoT edge nodes will need many more cost-effective multi-die ICs to process data locally and provide fast and intelligent responses to changing environmental parameters, system wear-out and/or operation changes required.
- Data and compute centers will continue and significantly expand how they leverage the enormous performance-per Watt advantages of multi-die ICs to cut their response times, operating cost, and space requirement.
- `A wide range of transportation and industrial equipment will utilize sensors, actuator, data converters, and digital functions, integrated in multi-die ICs, to reliably control power electronics, increase systems' efficiency, safety, and security.

While user-friendly operating systems and application-specific software will of course continue to gain importance in the semiconductor and electronic systems world, the interface to the real world – which in analog, highly complex, and continuously changing – demands cost-effective and reliable hardware, a.k.a. multi-die ICs.

Eliminating the Memory Wall

By Jan Vardaman, Techsearch International, Inc.

The adoption of 3D ICs allowed for the elimination of the "Memory Wall" using a new memory architecture and through silicon via (TSV) technology.

While individual ICs became faster with each process node, the communication between the chips was constrained by limited pin counts, power-hungry I/Os, and PCB-space limitations. Assembly of multiple die into onepackage enables extremely wide busses between them, shortens latency, and expands bandwidth between logic and memory, while cutting the power dissipation by up to two orders of magnitude.

The large memory vendors Micron (including Elpida), SK Hynix, and Samsung, as well as the specialty memory house Tezzaron, recognized this opportunity and already introduced DRAM "memory cubes." Combining multiple die in one high-pin-count package or die stack, they offer very large memory capacity.

By mounting such a memory cube on an interposer, side-by-side with a logic die ,or making them part of a 3D IC vertical stack, effectively elliminates the "memory wall".

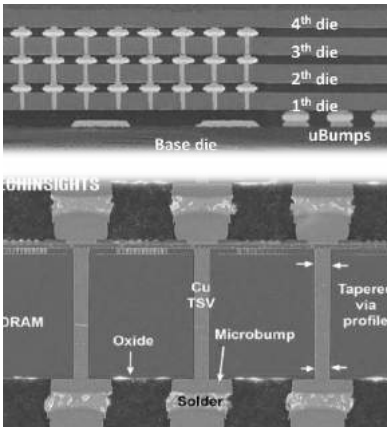


Photo Credit: SK Hynix

High bandwidth memory (HBM) is one of the most important 3D IC developments in the last 10 years. Over the last decade, stacked DRAM with TSVs has transitioned from a handful of research programs to rapidly increasing volumes.

Tezzaron has provided small quantities of 3D ICs for high-speed memory applications since 2005. Micron, Samsung, and SK Hynix began producing DRAM stacks with TSVs in late 2014 and early 2015.Micron began shipments of its Hybrid Memory Cube (HMC) in 2015. DRAMs and the logic controller were interconnected with TSVs. HMC was packaged in a ball-grid array (BGA) and tested before assembly on the board.

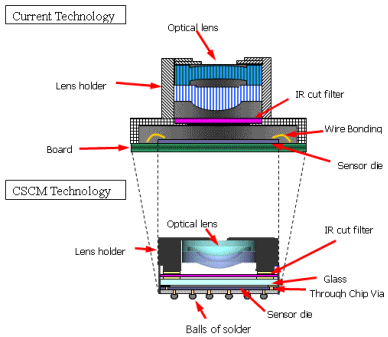
The HMC is used in Intel's Knights Landing. The silicon-on-insulator (SOI) logic layer was fabricated by GLOBALFOUNDRIES (which purchased IBM's fab) and the memory was fabricated by Micron.

Micron used a thermo-compression bond (TCB) process with a non-conductive film (NCF) underfill for its die stacking in the HMC.

From 3D Pioneers to 3D Robots

By Dr. Phil Garrou, IFTLE, Microelectronics Consultants of North America

It is clear to most of us who have been following the 3DIC area for the past decade plus, that the origins of this technology come from the early (1980s-1990s) work of Mitsumasa Koyanagi in Japan and Peter Ramm in Europe.[1] If you're asking what the defining event was that propelled it from obscurity to becoming a buzzword of the 2000's, I'd have to say it was the Toshiba announcement in Oct of 2007 of the production of the "chip scale camera module", which would revolutionize image sensor production as we knew it.[2]



The scientific community had agreed that true 3D IC would require (3) things: (1) chip thinning; (2) chip stacking and (3) connection through the silicon with the through silicon via (TSV). While thinning and stacking technology was already in production and only needed minor advancements to be used in 3D ICs, TSV was an obscure technology only used by some MEMS practitioners. The Toshiba CMOS image sensor announcement, with its backside TSV to significantly downsize the size of image sensors, brought this technology mainstream and caused the tidal wave of research and product introductions that were to follow. For those who don't remember these early days, this was the work of Kenji Takahashi.[3]

Where will 3D and heterogeneous integration technologies take us in the next 10 years? In reality, most can only predict the future in hindsight (and you can quote me on that). If you don't believe me check the market prognosticators projections for 3DIC adoption in the 2008-2012 timeframe. Some actually predicted that the first applications would be flash memory!

Right now, 2.5D/3D IC technology is still too expensive for adoption in standard consumer applications. Qualcomm and many others spent a lot of time and money trying to lower the price point, but in the end were not able to. It has certainly found a niche in stacked memory, FPGA modules and graphics modules, but those are high-end costly applications. Current predictions appear to favor future adoption in high performance computing (HPC) and artificial intelligence (AI), which seem to be logical applications, but we will see.

I certainly have been impressed by Sony who has burst to the head of the class in terms of image sensors, which now contain thinning, stacking and TSV. Sony management has indicated that they will require this technology to advance their robotics platform.[4] So… if I had to place a bet on my answer at this point, I would have to say robotics.

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[2] https://www.electronicsweekly.com/news/products/sensors-products/toshiba-image-sensor-camera-modules-2007-10/

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[4] http://electroiq.com/insights-from-leading-edge/2017/01/iftle-319-mike-ma-to-amkor-3d-asip-part-2-image-sensing-sony-tessera-smic/

Thank 2.5D Interposers for the Success of 3D ICs

By Mark Scannell, CEA-Leti

Would it be flippant to say that most pivotal event that impacted the commercialization of 3D integration technologies, may have been the commercialization of 2.5D technologies? Arguably, 3D and silicon interposer are very different technologies, with a common denominator that happens to be the through silicon via (TSV).

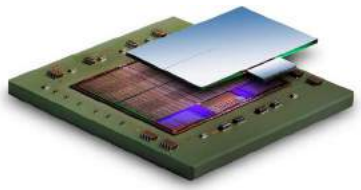
Until Xilinx announced its Virtix-7 2000T in or around 2011, skepticism was the other common denominator. 3D memory cubes were certainly in the ether at the time, but there was still much debate about the cost and commercial viability of TSV technologies.

Tasked as I was then with promoting 3D integration technologies, I was struggling to sell the larger picture of overall system performance benefit versus, say, the direct single-step cost adders such as metalizing a via or temporary

handling of thin wafers or other such 'inconvenient' processes.

Ironically, yield was an often-used argument to rationalize that the cost of 3D would always be prohibitive. The notion of known good die (KGD) was considered difficult to measure, and how to accommodate yield multiplications related to stacking, remained a sticky question.

Then suddenly, along comes Xilinx with their silicon interposer, of which the TSV cost adder was paid for by none other than yield enhancement. Rather than building a single, very low-yielding large 28nm chip, Xilinx 'simply' (I use the word loosely) built smaller and thus better yielding 28nm chips and assembled them on an interposer. The system performance benefit ended up being financed by the very same yield that was supposed to be the problem. I say Xilinx, but of course, TSMC deserve their share of the credit too.



For me this was a pivotal moment because suddenly the hypothesis that TSV technology would always be too costly to commercialize was clearly disproven. I must admit, I never anticipated that yield improvement would be the elusive initial justification for TSV integration costs – I was looking far and wide, and elsewhere.

So now, after publicly admitting that I never saw that one coming … I'm expected to look into the same crystal ball and have you believe that I can see what's coming next?

Well, for what it's worth …

The (very reliable?) crystal ball

Data generation, collection, analysis, storage and management (and dare I say abuse?) will continue to increase. Whether it's due to the famous Internet of (every and any?) things (IoT), autonomous driving, high performance computing or whatever, I think it's fair to expect there will always be a demand for improved performance (specifically memory bandwidth) with reduced energy consumption and reduced cost. Traditionally, in terms of timing, the improved performance leads and the reduced cost follows. I say that because it conveniently allows me to ignore cost for what I'm about to forecast (experience tells me all I have to do is hang around until a future Xilinx-equivalent comes up with that solution!?).

Quantum computing is certainly a hot topic but let's put it aside for the moment. As a rather pretentious professor once said to me; "there are two kinds of people – those who understand quantum mechanics, and those who don't".

I must admit, I'm attracted to die-to-wafer hybrid (D2W) (a.k.a. direct) bonding. The wafer-to-wafer version (W2W) works very well. It's my understanding that W2W hybrid bonding is more or less restricted to imager applications most likely due to the requirement that both dice must have the same size. D2W however removes the equal die-size requirement, which in theory could bring the performance benefits of hybrid bonding to almost any 3D system. And the performance benefits of hybrid bonding are not to be ignored: decreased interconnect pitch, shorter interconnects, faster communication, reduced loss, etc.

All of this sounds familiar because it's basically the justification for any interconnect improvement ever proposed, including TSV's back in 2011 – so it cannot be completely irrational to at least consider this approach (right?). D2W bonding could also enable, for the want of a better description, 'partitioned-systems' like the current interposer systems but with chiplets instead of chips, and active silicon interposers instead of passive ones.

Indeed, Intel has just announced its Foveros 3D integration scheme, which seeks to achieve competitive advantage by partitioning logic chips and stacking the resulting chiplets on top of each other. My organization, CEA, and others, such as DARPA, are also working on such initiatives.

Photo credit: DARPA

Of course, D2W hybrid bonding will require some further development and collaboration before being sufficiently mature for industrial scale chiplet integration. Whatever performance the chiplet programs are achieving today, or planning to achieve, one could assume that the performance would be further increased with hybrid bonding. The Foveros technology seems to be relying on face-to-face, 36µm pitch µ-bump interconnects. However, with hybrid bonding this pitch can be reduced to 5µm.

Many issues remain, not limited to dicing a perfect wafer surface (i.e. hybrid bonding requirement perfect!) in a way that the die surface is as perfect after dicing as it was before. Then picking and placing that perfect die surface on an equally perfect wafer surface with, by the way, very high alignment accuracy and high throughput. If Intel can live with the alignment accuracy versus throughput compromise of 36µm pitch interconnects, maybe we're not actually that far from a 5µm accuracy/throughput compromise?

We know that D2W is possible in principle, and D2W electrical results have been demonstrated to be as good as W2W results. In any case, there is no fundamental reason that the electrical results should be different.

We will need to develop a 'clean' dicing process along with some sort of auto-alignment system to fix throughput. Who knows, maybe the hybrid bonding with collective auto-alignment will end up being lower cost than, say, µ bumps + underfill or thermal-compression alternatives?

There you have it, my clear-as-mud crystal ball forecasts the introduction of D2W hybrid bonding at an industrial level, within 10 years …or thereabouts.

Heterogeneous Integration Calls for Increased Materials Reliability

By Dr. Andy C. Mackie, PhD, Indium Corporation

Automotive reliability is a pivotal concern for heterogeneous integration technologies, especially as emerging mission profiles for electric and autonomous vehicles push component lifetimes out by two to three times or more over standard testing regimes. There has been increasing realization of the importance of chip-package interaction (CPI) as a source of reliability issues in semiconductor assembly. Pinning it down to a single date as the key event, the release of JEDEC JEP156A in March 2018, was a good start in this direction, as it shows a major deviation from the old but still useful Arrhenius/activation energy kinetics models.

Exacerbating the problem is the fact that coreless and thin substrates, thin (2.5D) interposers, and large thinned die have become prevalent in the advanced processor market; there is no single "solid/inflexible" part of the package against which everything else moves. Therefore, the thermal and mechanical stresses present are mutually interdependent and advanced stress modeling and increased understanding of CPI failure mechanisms will be needed.

Heterogeneous integration is here to stay for a few reasons. First, it allows a more modularized approach to system design. Rather than original equipment manufacturers (OEMs) having to ask subcontractors for a specific component or a named device, they can provide a pad layout design and desired functionality and device dimension to their suppliers and ask for that in 18 months.

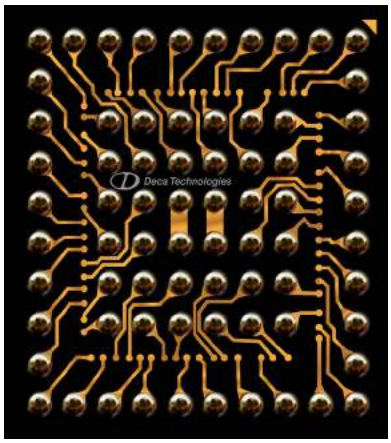
Secondly, there is no longer a need to rely on specialty system-on-chips (SoCs) so you don't have the headache of building mixed technologies (like Si and III/V) in the same tool. At SMC 2018, Micron's John Smythe put this as "running peanut butter in a chocolate fab."

Finally, if dies are built separately then packaged together, well-characterized fabrication processes will lead to high-yield for individual die; and known-good-die are then used in the final assembly.

When it comes to wafer-level packaging (WLP) and panel-level packaging (PLP), there are still many issues in fan-out PLP co-planarity for larger packages. The need for technologies such as Deca Technologies Adaptive Patterning™ pad registration software is a tacit acknowledgment that polymer cure in these advanced packages needs much more attention than is presently being given.

We can expect to see near-term developments in modeling of the polymer curing process, and specialty heating systems being developed as a result, especially for the huge panels (>50x50cm) being discussed in various consortia.

Higher frequency RF devices will be especially sensitive to any deviation from the original I/O layout. For ball-attach on these packages, specialty fluxes have been developed that eliminate many of the emerging failure modes seen with the thin copper traces on the redistribution layer.



The use of wide I/O memory stacks on 2.5D substrates for advanced processor applications needs strong, reliable solder joints. Although the memory dies themselves are being increasingly stacked using non-conductive film by Southeast Asia memory manufacturers, a very low-residue no-clean flip-chip flux is now extensively being used for memory stack attach onto the 2.5D interposer.

Extending Moore's Law through Advanced Packaging

By Carl McMahon, Genmark Automation

The performance and productivity of microelectronics have increased continuously over the last 50 years due to the enormous advances in lithography and device technology. Today, these technologies are becoming prevalent in 3D packaging, which further enables advances in integrating various technologies (logic, memory, RF, sensors, etc.) in a small form factor.

There are concerns with the sustainability of shrinking devices beyond 5nm and the costs associated with it. Advanced packaging compliments current technologies, which in turn allows 'Moore's law' to extend for several generations.

From Genmark's perspective, guid-

ed by over 30 years of experience, the migration to Si or Si-type substrates for 3D packaging allowed much of current semiconductor technology to be adapted for their processes. This is particularly true for automation, where mainstream automation designed for integrated device manufacturers (IDMs) can be modified for substrates used in 3D wafer-level packaging (WLP).

Data from Genmark show that 10 years ago, we sold to companies who were working on developing more efficient, cost-effective, high-volume 3D packaging technologies. Since then, we have been involved with these and many other companies at the forefront of packaging. Companies and research institutes worldwide have demonstrated 3D integration processes. Genmark's development of the CODEX stocker to serve the glass wafer segment of the market was driven by the need to lower costs and improve performance for WLP companies.

Cleanliness requirements in advanced packaging is now similar to any of the leading-edge IDM companies. However, in the area of substrate handling lies some of the most difficult challenges because the exclusion zone for substrate handling is greatly reduced. This, in turn, has led to the rise of 'no-touch' end effectors, based on Bernoulli principles. Genmark is one of the very few companies that can run a 100% 'no-touch' handling process on to panels up to 450mm. The focus for us now is to work with our customers on improving throughput and performance of these technologies, ultimately enabling the production of more cost-effective products.

Looking forward to Genmark's next 10 years, the recent acquisition by Nidec-Sankyo gives us the ability to provide our technologies across a broader range of companies. Nidec-Sankyo has a global reach and technology platforms that Genmark can leverage to constantly innovate new solutions within the 3D packaging space.

We see requirements for 'smarter' handling solutions, building 3D software models of applications before releasing to the customer. Developing the applications 'virtually' can speed up product launch to an industry that has no established single substrate size. Coupled with this are both thickness and material type challenges which requires novel handling regimes. Nidec-Sankyo's teams and Genmark's together have already created new handling technologies which will benefit all of our advanced packaging customers.

10 Years of Invent, Innovate, Implement at EV Group

By Françoise von Trapp

Left to right, Clemens Schütte, Werner Thallner, Françoise von Trapp, Herman Waltl, Paul Lindner, and Thomas Uhrmann.

Of all the companies that have supported 3D InCites over the past 10 years, none has been more consistently involved, both as contributor and sponsor, as EV Group. In fact, without EVG's belief in our mission and their sponsorship the first three years, 3D InCites would not exist today. Therefore, it seemed fitting to honor them with the cover story for this 10th anniversary edition.

Since the beginning of 3D integration, EVG has been there. They were the first to invest in R&D for image sensors. They implemented the first fusion bond and the first layer transfer for sequential 3D stacking.

The inventors of temporary bond/debond (TB/DB) processes, their solutions are as old as the market, back when they were referred to as tape mounting systems, notes Paul Lindner, executive technology director at EV Group.

"We are a technology provider," he said, "The equipment industry has to be. There are no high-performance chips without the right tools." Additionally, he said, it takes a combination of processes, materials, and equipment to achieve success. The burden of optimizing those processes falls to the tools. "Equipment has to continually improve and optimize," said Lindner.

Visits to EVG Headquarters

In the past 10 years, EVG has grown exponentially. I have been invited to tour the ongoing expansion at corporate headquarters in Schärding, Austria four times. The first time was in 2010; the year of the company's 30th anniversary. I returned in February of 2012, January 2014, and most recently in November 2018.

Since 2009, the manufacturing area grew from about 3,100 to 7,100m^2, the machining center from approximately 1,900 to 3,600m^2, and the cleanroom area from approximately 1,200 to 2,800m^2, says Clemens Schütte, director of marketing and communications.

In the same period of time, the number of employees worldwide increased from 430 (Sep 30, 2009) to more than 860 today.

EVG Expansion Timeline:

2011

Manufacturing II for final assembly

2012

Cleanroom IV

2013

EVG Minis kindergarten / childcare facility and INNside restaurant

2013

New office building and reception area

2016

Machining Center II

2017

New test room building

2018/19

New Manufacturing III building

Werner Thallner shows me around the construction site for EVG's latest expansion, called Manufacturing III.

Triple I Today – November 2018

My most recent visit to EVG included a construction site tour and lunch with members of EVG's leadership team including Werner Thallner, Paul Lindner, Hermann Waltl, and Thomas Uhrmann, as well as Clemens Schütte and Klaus Doblmann from the marcom team.

In the four years since I last visited EV Group, a new machine shop and test room building were added. The new machine shop was built around the old one, doubling its size to 3600m^2. It features a new CNC milling machine large enough to machine parts that larger tools require for handling a variety of substrate sizes, such as for panel level packaging for fan-out wafer level packaging, or flat panel displays.

On this particular day in the class-1 clean test room, a next-generation fusion bonding system (Gemini FB XT) configured for hybrid bonding of image sensors and stacked flash memory was being put through its paces. This tool features cleaning and plasma activation modules used for preconditioning wafers before bonding, and the latest SmartView NT3 aligner, its alignment accuracy has been improved from 500nm to 50nm; That's 10X in 10 years.

"That's better than Moore's Law," noted Thallner. "While speed and accuracy are both important for 3D and we are working on both, alignment is more critical. Verification of alignment directly after bonding is critical for high yield too. We are the only company that offers alignment verification integrated in the fusion bonder."

Two robots keep the wafers moving. The floor in the test room is raised so that connections can be made under the floor.

The latest construction, dubbed Manufacturing Building III, will connect manufacturing with final assembly and test so that there is no need for customers to walk outdoors. In addition to expanded manufacturing and warehouse space, there will be a designated packaging area designed specifically for cleanroom equipment. Shipping and receiving will be centralized in a restricted area, as the company is authorized to inspect tools for shipping.

In Growth Mode

These days, the company is fully immersed in all aspects of heterogeneous integration. Its tools and processes support all the elements of bonding and lithography.

More than Moore is on the rise, says Lindner, and the company's

Markus Wimplinger shows Françoise von Trapp a 300mm bonded wafer on tape carrier.

Excerpt from "Triple I" at Work – September 8, 2010

EV Group sums up its philosophy and mission in three words: "Invent, Innovate, Implement". Whatever market EVG enters into, the company's goal is to be the first to explore new techniques and serve next-generation applications of micro and nano-fabrication technologies. The list of industry firsts supporting this is long and includes such notable achievements as developing the first backside lithography system for MEMS, the first wafer bonding systems that would set the industry standard, the first nano-imprint system, and the first automated SOI bonding system. As Hermann Waltl, executive sales and customer support director, pointed out, the "Triple I" philosophy isn't merely a marketing tagline – at EVG it's a way of life and the company's secret to success.

Excerpt from Triple I at Work, The Sequel: February 2012

With such a banner year under their belt, the promise of steady future growth, and the desire to ramp up the company's status to that of a Tier 1 supplier, it was time to pull out the plans to expand the facility.

According to Werner Thallner, executive operations and financial director, advanced planning to design the expansion and secure government approval and building permits allowed for rapid implementation of the project once they pulled the trigger. "Literally, about one hour after I made the decision to ramp up and build the building, the builders arrived and started building the building. Within 4 ½ months – on December 1, we moved in and began production."

The newly constructed four story building with two-story manufacturing floor doubled the size of the current manufacturing space and meets the cleanliness requirements of a Tier 1 manufacturer (class 100K). Additionally, the building features an overhead train to make it easier for moving tools around, and hydraulic ramps to make it easier for technicians to work on the tools, thereby improving the working conditions.

Thallner also said that integrated test rooms were built that can go down to Class 1K. With the test rooms, the concept was to separate testing from manufacturing to address the security needs of customers to split up technologies of different customers to prevent them from seeing what each other is doing.

Paul Lindner shows Françoise von Trapp a 450mm wafer used to test its 400mm SOI wafer bonding platform.

Manufacturing II for final assembly and cleanroom IV expansions.

The new manufacturing floor in action.

Triple-I approach – Invent, Innovate, Implement – is paying off as all the markets they touch are in growth mode, from advanced fan-out wafer level packaging (FOWLP), interposer and 3D integration, to compound semiconductors and MEMS, photonics, biotech, and flat panel displays.

"It's been a long journey from the first lithography line for 3D packaging to industry adoption; a lot longer than we expected," noted Lindner. "And the nano-imprint lithography business took more than 15 years from invent to implement. It's important to start as early as possible and scale the process. You can't make a 'side entry' into a market when it ramps to high volume and expect to succeed."

For example, the company has more than 20 years invested in TB/DB R&D and has been through all the technology changes, from thermoplast and mechanical debonding, to zone bond invented together with Brewer Science. The different TB/DB methods suit different applications, and EVG supports them all.

Submicron Accuracy Bonding

EV Group is perhaps best known for its advancements in permanent wafer bonding tools, where it is a market leader.

Uhrmann says new application drivers like artificial intelligence and machine learning require high levels of computing at the edge and cloud. This calls for high-density interconnects that are bonded at pitches of 2µm or smaller. As a result, interest is growing for fusion

The latest CNC machining tool is twice the size of the other machining tools in EVG's machine shop.

Excerpt from The EVG Story Continues... February 2014

Paul Lindner, EV Group's executive technology director, filled me in on what's new since my last visit in 2012, such as the 21000m² addition that includes new offices, double the cleanroom space, a training center for internal and customer training, an R&D center specifically for new tool design and developments, an on-site restaurant for employees and an on-site kindergarten.

Additionally, they upgraded the older cleanrooms to a newer standard and class-10 cleanliness to make them state-of-the-art and closer to what customers are running with regards to temperature and humidity control.

The idea, explained Lindner, is to produce process results equivalent to customer operations, and is driven so that they can create more automated systems that accurately determine known throughput and cost of ownership (CoO). EV Group has also grown its international footprint, with EVG China and EVG Taiwan now fully established to serve those regions with increased process support and technical support for its install base.

The new kindergarten and Innside restaurant.

and hybrid bonding processes.

Understanding the growing importance of alignment accuracies for fine-pitch applications, its latest-generation SmartView® face-to-face bond alignment system features 50nm alignment.

Armed with the SmartView NT3 system, EVG's flagship automated fusion bonding system, GEMINI® FB XT, supports applications requiring higher alignment accuracies, such as memory stacking, 3D systems on chip (SoC), back-side-illuminated CMOS image sensor (BSI-CIS) stacking, and die partitioning.

The company's latest tool introduction, the BONDSCALE™ automated fusion bonding system, is designed to support a broad range of fusion/molecular wafer bonding applications, including engineered substrate manufacturing and 3D integration approaches that use layer-transfer processing, such as monolithic 3D (M3D). With this tool, EVG brings wafer bonding to the front end.

Paul Lindner explains the features of EVG systems. (L-R) Lindner, Clemens Schütte, Françoise von Trapp, Hermann Waltl.

In addition to wafer-to-wafer hybrid bonding, EVG is also working in collaboration with imec to develop wafer-to-wafer processes, to be able to increase throughput, in addition to achieving 50nm alignment accuracy.

The Road to 3D TSV Adoption

After lunch, Uhrmann and I sat down to reminisce about the past 10 years, and specifically the longer-than-predicted road to 3D TSV adoption. Beyond the well-known cost challenge, there were other technology issues that delayed progress.

One of the biggest challenges was regulating the keep-out zone around devices to reduce impact of TSV-induced stress. "Managing the stress in a 3D wafer is not a piece of cake," noted Uhrmann. Bow and

Chatting with Paul Lindner, Werner Thallner, and Hermann Waltl in the new manufacturing area.

Checking out the EVG850TB/DB XT HVM temporary bond/debond system in action.

Excerpt from Triple I Prevails at EV Group – February 2014

We took a group tour of the new class 100 cleanroom, where I was able to see some of the tools we'd discussed in action. For me, since I had first seen the first prototype of the EVG850TB/DB XT HVM temporary bond/debond system on the manufacturing floor when I visited in 2012, seeing the same tool in action in the cleanroom completed the story for me. The fact that it also won the 3D InCites Award for equipment made it that much more exciting.

Markus Wimplinger, corporate technology development and IP director, put the tool through its paces, demonstrating the high throughput operation with 9 process modules. The in-line metrology feature for inspecting adhesive thickness is probably one of the coolest features of this tool, because it can quickly measure up to 300,000 separate points on a wafer, which delivers more accurate results with more data to help in process optimization. "It's critical to scan at very high resolution. You can fool yourself about total thickness variation (TTV)," explained Wimplinger. "Ours is the only one that can measure 100% of the wafer at high resolution in less than 90 seconds."

strain caused by how the wafers react to copper called for process adaptions for the whole fab supply chain, from substrate changes to etching and deposition processes, to debonding methods.

Did the development of FOWLP slow down progress for 3D TSVs? Uhrmann says no. To the contrary, he says he thinks fan-out technologies put advanced packaging – including 2.5D and 3D TSVs – on the prime stage. It became clear that heterogeneous integration through advanced packaging was the way forward to achieve more functionality and performance.

The semiconductor industry is notoriously slow to adopt new technologies. As long as 2D approaches worked, there was no reason to change, explained Uhrmann. It wasn't until there was no other way to achieve performance requirements, that 3D TSV was adopted. Uhrmann credits the smart phone — and particularly the iPhone 3S — for ramping BSI-CIS into volume production. Next came memory stacking, using TSVs in DRAM stacking to achieve high-bandwidth memory (HBM), but that took longer to achieve.

Small devices, such as smart phones, changed the entire industry. And now artificial intelligence that enables cloud and edge computing are driving performance requirements even higher, while also driving down-power requirements.

"This is what is pushing advanced packaging. We need flexibility that you can't get with just chip design," says Uhrmann. "It's not just about logic anymore, it's all about systems. Advanced packaging is how you smartly connect dies. 3D will be everywhere for More than Moore technologies." When that happens, you can be sure EVG will be ready for it.

Werner Thallner joked that the new building is connected to the old one using "through concrete vias". "That's bonding in action."

Advanced Heterogeneous Packaging Solutions for High Performance Computing

By Ron Huemoeller, Mike Kelly, Curtis Zwenger, Dave Hiner, and George Scott, Amkor Technology, Inc.

Heterogeneous integrated circuit (IC) packaging has made a full entrance into the high-performance packaging arena. The target applications are broad, running the gamut from artificial intelligence (AI), deep learning, data center networking, super computers, and autonomous driving. In fact, a new generation of deep learning AI, leading central processing units (CPUs) for datacenter servers as well as new performance-leading CPUs for the latest blade servers have literally been made possible by these remarkable IC package constructions.

These cutting-edge technologies are leading the way for incredible advancements. Moreover, they all have a common characteristic: high-speed, high-performance ICs.

Investment agency Goldman Sachs Group has predicted that global AI hardware microchips including CPUs, graphics processing units (GPUs), application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs) and others, will grow at an annual compound rate of more than 40% in the coming years (Figure 1).

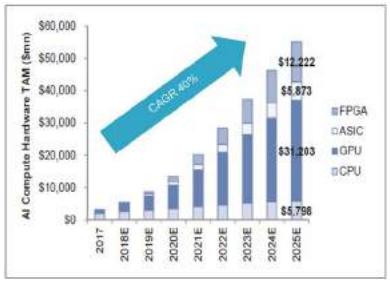


Figure 1. Worldwide AI computing hardware total available market (TAM). Source: Goldman Sachs 2018

In deep learning, continuous advancements in algorithms and big data accessibility combined with high-performance compute engines based on heterogeneous IC packaging are driving the giant leap forward for this technology wave. The package construction has permitted a two-fold leapfrog in what was possible previously, specifically: a memory bandwidth improvement thanks to high bandwidth memory (HBM) introduced by Samsung and Hynix, and the ability to provide more off-package signaling capacity.

HETEROGENEOUS PACKAGES HAVE OVERCOME THE EXISTING LIMITATIONS OF MONOLITHIC INTEGRATION AND SIGNIFICANTLY INCREASE THE CAPABILITIES AND PERFORMANCE OF TODAY'S ELECTRONIC PRODUCTS.

Heterogeneous Packaging Approaches

FCBGA MCM

Heterogeneous digital integration using flip chip BGA (FCBGA) packages has been occurring for years and the variety of approaches has been nearly endless. The intra-die routing capability for multichip modules (MCMs) is good, and as long as the layer count to achieve this can be accommodated, it will continue to be a viable approach for many devices.

TSV

Through silicon via (TSV) development took several years to perfect in silicon interposers but really ushered in the modern heterogeneous surge. The implications were profound, as the highest bandwidth DRAM (HBM) available were designed exclusively for silicon interposer applications. This new performance level was only available in 2.5D TSV packages:

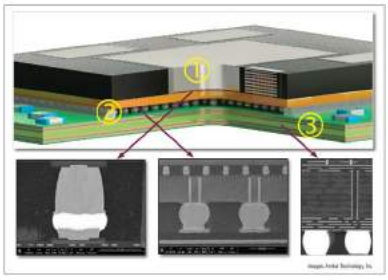


Figure 2. Three key elements of advanced 2.5D packaging technology

first in ultra-performance graphics, then deep-learning accelerators and now in datacenter networking switches and server CPUs. The main requirement for silicon interposers is that the HBM device uses an ultra-wide 1024-bit parallel bus requiring signal routing traces of 2µm width or smaller. This is 8-10 times the routing density of an FCBGA substrate.

Amkor's TSV reveal process and chip-on-wafer (CoW) packages have been in high-volume manufacturing (HVM) for three years. The assembly processes are high-yielding flagships of the new ultra-clean K5 facility in Song-Do, South Korea, near the Incheon International Airport. Figure 2 shows the key elements of a typical implementation of this packaging technology.

HBM: Just the Beginning

Processors used in conjunction with HBM in 2.5D TSV packaging constructions came first, but this is viewed as just the beginning. Today, the expense of 7nm and upcoming 5nm design will sharpen the focus for the content placed into the system-on-chip (SoC), ASIC or the processor. Leading

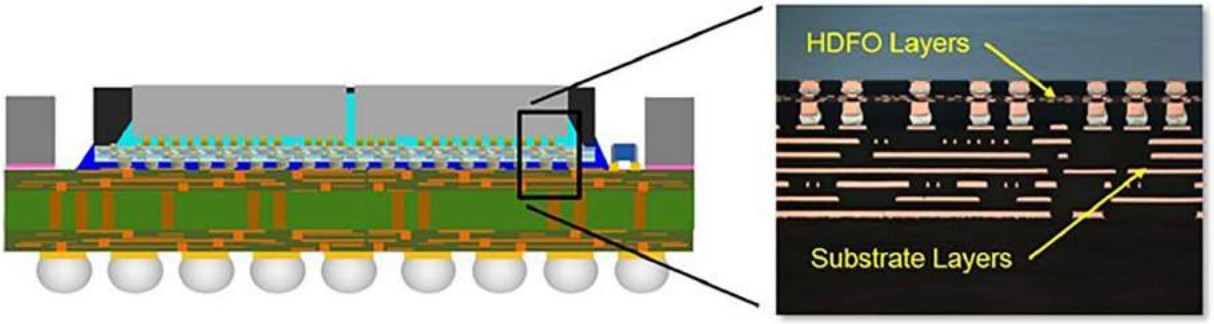


Figure 3: A high-density fan-out solution

advancements beyond single SoC approaches are in-package combinations of the processor and multiple discrete I/O die and even multiple processor chips in an effort to increase the core count and discrete I/O die. Several current examples of these have been prototyped and announced.

One of the key intersections between new levels of device performance and heterogeneous IC package structures is the intra-die signal routing capability. The 2.5D interposer offers a copper back-end dual-damascene technology with excellent fine-line capability and reasonable electrical signaling performance for short runs. Today, 2.5D TSV is the proven path for HBM integration into your product designs.

Another up and coming technology uses the so-called "dies-last," high-density fan-out (HDFO) approach.

HDFO Packaging

HDFO packaging is being developed as another crucial pillar for heterogeneous integrations to lower the cost of high-performance heterogeneous applications. This fine-line redistribution layer (RDL) approach is capable of 2µm line/space and 4-layer counts to provide the inter-die routing. In this case, the copper/organic dielectric RDL layers are fabricated on a glass or silicon carrier and then the wafer is populated with functional die and molded in a manner very similar to 2.5D designs (Figure 3).

For the 2.5D package design plan, the design flow and design methodology are very different from traditional package designs. For example, an HBM2 DRAM having 4,000 bumps, and a main chip maybe having tens of thousands of bumps and multiple chips, are connected through an interposer. To do this, the design, simulation for optimization, and rule-checking need to advance. Addressing these challenges, Amkor has already developed outsourced semiconductor assembly and test (OSAT), industry-leading process assembly design kits (PADKs), and a design flow to achieve electronic design automation (EDA) connectivity with Cadence and Mentor Graphics.

The kits are introduced during the design stage and achieve a synchronous debugging design environment to carry out comparisons between schematic and layout diagrams and to perform all design rule checks (DRCs). This process achieves rigorous design verification and sign off. In addition, by extracting the design, interposer and substrate models, and implementing co-design and co-simulation, design-for-performance (DFP), design-for-cost (DFC) and design-for-manufacturing (DFM), are also achieved. Figure 4 shows one example of a simulated eye-diagram, with the HBM data bus operating at 2 GHz frequency.

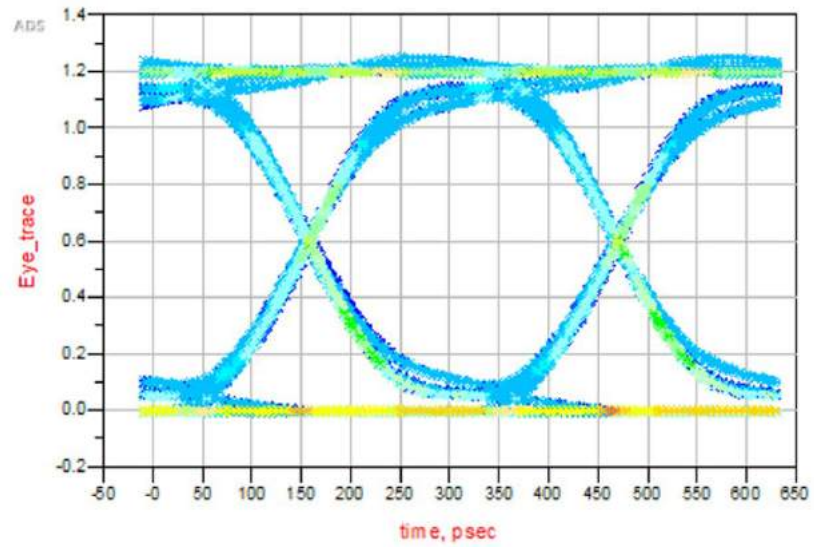


Figure 4. Eye diagram showing the performance of co-packaged ASIC and HBM2

Summary

Heterogeneous packages have overcome the existing limitations of monolithic integration and significantly increased the capabilities and performance of today's electronic products. As silicon integration faces additional and even more difficult challenges, the next step towards heterogeneous packaging will fulfill an even greater role to take end products to ever higher levels. The packaging solutions are available today to make the next generation products a reality.

CoolCube™: Much more than a True 3DVLSI Alternative to Scaling

By Jean-Eric Michalette, CEA-Leti

Almost four years ago, we published an article titled "CoolCube™: A True 3DVLSI Alternative to Scaling" on 3D InCites. It described the concept of stacking layers of transistors sequentially on top of each other and documented the research effort happening at Leti to develop a feasible process integration scheme and a comprehensive product design frame. Now, four years later, we can say that pioneering this concept has put Leti in a very good position to lead the next few decades of innovation in microelectronics.

In reality, the limits of 2D scaling described three years ago remain, and are even more present than before, calling for a new approach that includes 3D capabilities. Fewer than four fab companies are producing 2D technology below 10nm. Cost-of-ownership for those nodes are skyrocketing to such levels where only a few ICs can assure a return on investment. Even if several applications require such advanced technologies, most companies are now looking to enable innovative 3D stacking flows (Figure 1).

For systems requiring high performance, advanced 3D technologies such as hybrid bonding and monolithic 3D are considered to be the only ways to push computing to higher levels, given desired targets for memory capacity, memory bandwidth, power efficiency, reliability, and cost. For systems requiring heterogeneous applications, those technologies provide multiple opportunities to enable efficient edge computing of sensor data.

Towards 500°C device, and below

3D sequential integration aims to provide a concept for stacking devices with a nanometer scale resolution, allowing low aspect ratio and small 3D-contact fine-grain interconnects. It requires limiting the thermal budget of the top tier processing to a low temperature (less than 500°C) to ensure the stability of the bottom devices.

Leti's 3D sequential integration concept is called CoolCube™. After more than ten years of research, Leti is now able to present breakthrough proof points in several areas that were previously considered as potential showstoppers for 3D sequential integration. Either from a manufacturability, reliability, performance, or cost point of view, on a 300mm FDSOI advanced platform, experimental data from Leti has now demonstrated the ability to obtain:

- Low-resistance poly-Si gate for the top field effect transistors (FETs)
- Full low-temperature raised source and drain (LT RSD) epitaxy including surface preparation
- Stability of intermediate back-end-of-line (BEOL) between tiers with standard ultra-low-k (ULK) copper (Cu) technology
- Stable bonding above ULK
- Efficient contamination containment for wafers with Cu/ULK intermediate BEOL, enabling their re-introduction into the front-end-of-line (FEOL) for top FET processing
- SmartCut™ process above a CMOS wafer

Leti's work has focused on functionality demonstrations of the

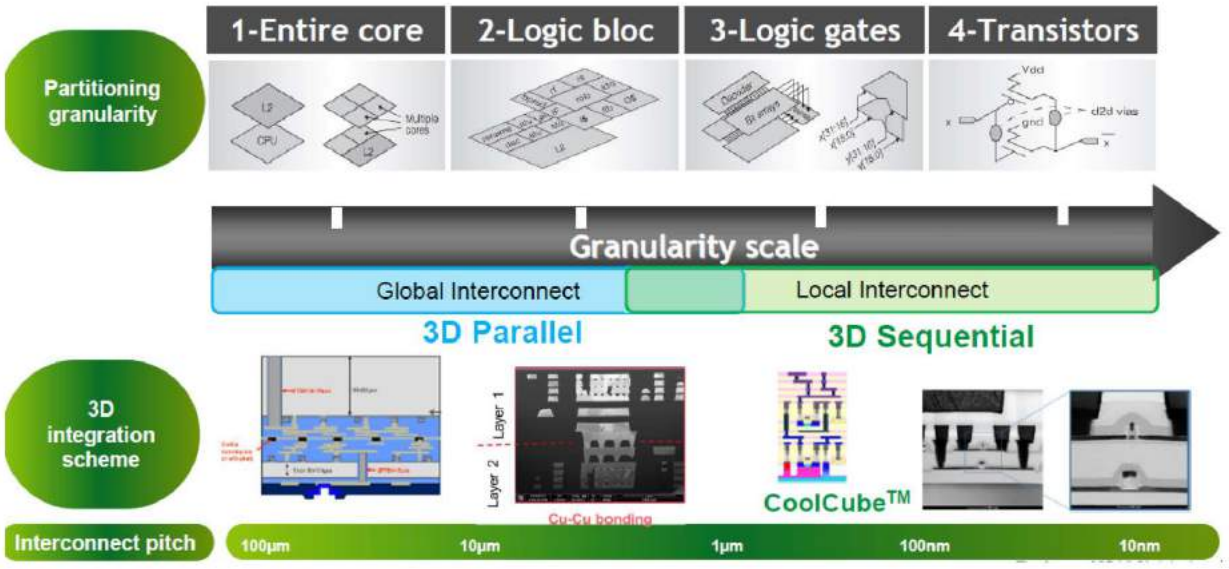


Figure 1: Two 3D VLSE complementary approaches by CEA – Leti

CoolCube concept. However, some performance measurements already enable validation of the concept for certain electrical device specifications:

- At 500°C, compared to a high-temperature process scheme, no degradation of bottom MOSFETs has been measured.
- On 2D readout and on 3D full stacking, we demonstrated the capability to form the junctions at low temperature without any performance degradation (Ion, Vt) for the top layer N or P devices. Slight degraded values are not due to mobility but to access resistance, something greatly improved by replacing the nitride spacer.
- For bottom level transistors, we observed no change in terms of reliability. Top level transistors meet lifetime requirements at 5 and 10 years, additional gate stack solutions investigated on short-loop lots are promising to improve the reliability level to be measured on the full-3D CoolCube (Figure 2).

Leti generated a portfolio of almost 50 patents around the CoolCube concept, the first one issued in 2008. However, Leti is no longer the only technology research organization working on 3D sequential integration. NARLAB, located in Taiwan; and imec, in Belgium, are also presenting papers on this subject at major conferences, increasing momentum of the concept for the future of microelectronics.

Cost Figures

Beside process integration research, Leti has also studied the cost figures of 3D sequential integration. If such integration is widely seen as a technological push, the economic benefit is not evident.

Most initial reactions towards this concept is to anticipate a clear drawback for digital applications: complexity factors, doubling expensive process modules, doubling lead-time, etc.

To establish parameters, Leti developed a unique analytical cost model to benchmark any technology node or 3D integration scheme compared to 2D. Based on die area, yield and mask count, this model considers benefits of the concept including time-to-market,

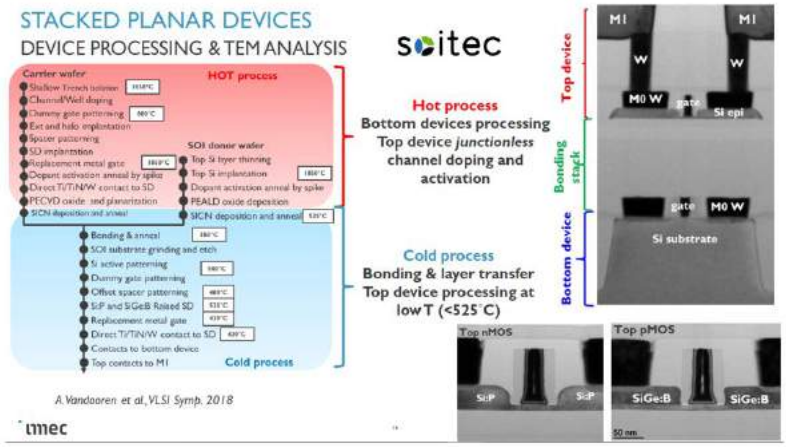


Figure 2a: Stacked planar device processing and TEM analysis.

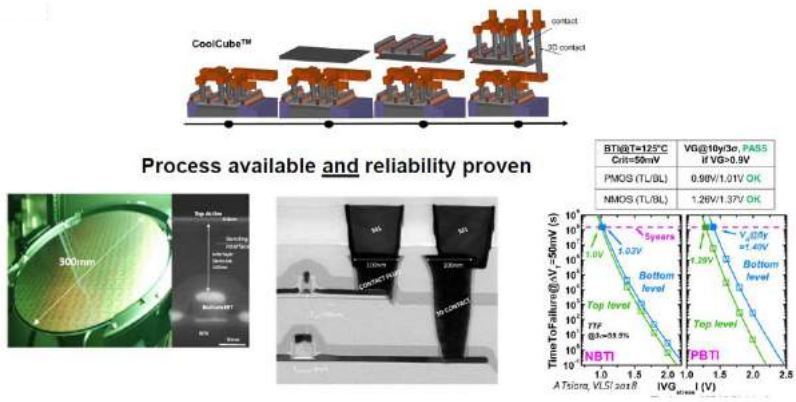


Figure 2b: 3D sequential integration: the ultimate vertical density

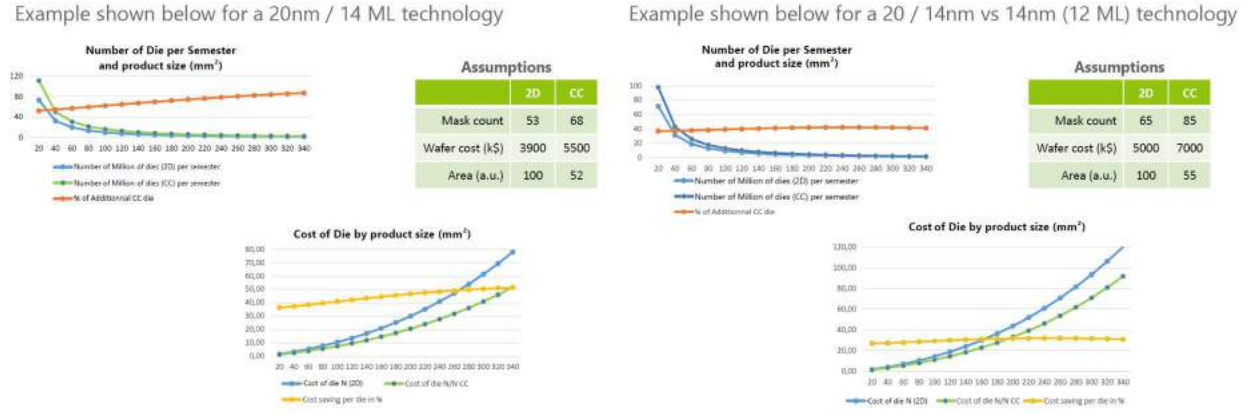


Figure 3: The model shows for digital products based on homogeneous stacking of N/N nodes that 3D sequential integration provides significant cost savings

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volume ramp-up, or new functions integration.

A main outcome of the study reveals that smart tiers/blocks/functional partitioning will be key to fully benefit from 3D sequential integration without any design evolution or circuit architecture changes.

Re-using 2D standard IP blocks and depending on the applications, there is a need to structure top and bottom tiers following the different block configurations:

- Data IPs (computing path), Memory (SRAM/ROM): High performance but wire congestion
- Clock tree: Keep accuracy and good circuits placement, very sensitive to BEOL loading
- Logic I/O, Analog/RF and passive: Dedicated process options required
- Service functions (as test / power management): Less performance-driven but close imbrication with Data IPs

For evaluation, two main implementations are tested: Node N over Node N and Node N-1 over Node N. Both implementations are compared to a 2D Node N configuration. Although it exhibits additional process complexity with an impact on yield or cycle time, for example, for digital products based on homogeneous stacking of N/N nodes, the model shows that 3D sequential integration provides significant cost savings (Figure 3). These savings are essentially due to the area reduction and the increased number of dies per wafer. From one node N to another, slight variations of the results are obtained but the trend is the same. Reusing validated IP on older than 28nm nodes is compatible with advanced node 3D integration and shows both cost saving and dies supply improvement.

We also recognize that 3D sequential technology is suitable for applications that require heterogeneous functions. Smart partitioning between the two devices layers may reduce process options and save cost.

Mixed-signal applications such as smart sensor, actuator, and interface (visible and IR imaging, nano electromechanical systems (NEMS) array, and LED) are particularly interesting; 3D HD interconnects (MIV) and fine-grained partitioning drastically reduce the footprint and save power.

3D sequential technology is also very promising in computing systems. In this case, the partitioning can be done between logic and other hardware IPs such as SRAMs, rapid IOs, signal converters, test infrastructure, and power management.

A complete EDA environment to design 3D test chips on CoolCube technology

During the last four years at Leti, a 2-layer technological and application design environment has been developed to design and fabricate real circuits as demonstrators of this 3D sequential integration. The recent H2020 3D-Muse project lead by Leti started in January 2018. It will allow us to deliver a first proof of concept.

CoolCube devices and MIVs are inserted between the M4 and M5 metal levels in a standard 10ML 28nm FD-SOI process from ST-Microelectronics. A unified design environment based on an incremental technology data base (ITDB) framework is available to design test chips in a routine multi-project wafer (MPW) at ST Microelectronics' advanced fab. Both the active layers and the whole metal stack are managed using similar tools and methods already well-known in 2D design: spice models, pcells, design rules check (DRC), layout versus schematic (LVS), parasitic extraction (PEX) of both layers, and global post-layout simulation (PLS) (Figure 4).

Spice models use data measured acquired on CoolCube process development engineering lots. Both 28nm FD-SOI and CoolCube technology stacks are merged to perform technology computer aided design (TCAD) simulations and to align top layer RC parameters extracted at the design level using Mentor Graphics Calibre XACT tool.

On the CoolCube layer, a standard-cell-based digital design is available using classical logic synthesis (Synopsys DC-Compiler 1-2016.03) and place and route tools (Cadence Innovus 16.20). In the context of logic on IPs (SRAMs or other) MIVs are managed automatically by the tools (power distribution from thick metal layers to bottom IPs, signal interconnects between bottom IPs and top standard cells). 36 standard cells are today available, allowing a first routine circuit design:

- Inverters: IVX9, IVX18, IVX35, IVX71

Figure 4: The CoolCube design process flow (L). Who does what in the collaboration with Leti and ST Microelectronics

- Buffers: BFX9, BFX18, BFX35, BFX71
- Logic gates: NAND2X7, NAND3X5, NOR2X6, NOR3X4, XNOR2X9, XOR2X9, AOI12X6, AOI211X9, AOI22X6, OAI12X6, OAI211X11, OAI22X6
- Flip-flops: SDFPQX9, SDFPRQX9
- Balanced cells: CNIVX10, CNIVX21, CNIVX41, CNIVX62 and latch: CNHLSX10 for gated-clock tree
- Decoupling cells: DECAP8, DECAP16
- Filler cells: FILLERPFP1, FILLERPFP2, FILLERPFP4, FILLERPFP1-CO3D, FILLERPFP2-CO3D, FILLERPFP4-CO3D;
- Well-tap cell: FILLERSNPWP-FP4_GP are available including classical views for P&R, Verilog and spice simulation, ATPG…
- A first set of I/O pads compatible with CoolCube is also available to build an I/O ring and develop any test chip in a package

The common ground plane is used to adjust the threshold voltage after fabrication; specific fillers (FILLERPFPx-CO3) ensure DRC clean design when the ground plane is opened due to the presence of MIVs.

Design flows and methodologies

Since the article we published four years ago, the Leti design team has also worked on a set of methodologies to properly design a circuit using the CoolCube concept. For a PLS and PEX module, a deck of MIPT format files is available that contains the description of the top-level stacking (FEOL/BEOL), bottom level considered as substrate (emulation), and also includes technology information such as metal resistivity, contact resistance, etc. and corner type.

The output is a netlist including resistor-capacitor (RC) parasitic elements and standard cell characterization. CoolCube circuit design uses signoff 2D tools, reuses 2D power mesh and clock tree, and co-optimizes cell density from one tier to the other. Digital flow & CAD tools are regular tools such as:

- Synthesis flow using Synopsys DC Compiler with LIB & DB files (function/timing) and cell characterization (based on spice simulation with layout)
- Place and route flow using Cadence Innovus with LEF techno (techno and routing information including MIV rules), QRC techfile (3D stacking definition, RC data generated from ICT file) and LEF files (SC layout abstract view)

A first evaluation has been done to compare thermal performances of different 3D technologies, something that is always put forward when we talk about 3D. To compare TSV+µ-bumps, hybrid bonding and CoolCube, we use a simple method that defines a representative set of experiments, different technology parameters (number of layers, 3D interconnection pitch, materials, etc.), a different power scenario, and thermal dissipation scheme. The thermal model used is the SAHARA tool from Mentor Graphics. The results show a better thermal coupling for hybrid bonding and CoolCube, a reduced hot-spot effect, but also a strong sensitivity to interconnect density and die thickness.

A second MPW was launched to examine multi-tier embedded memory / multiple array on periphery

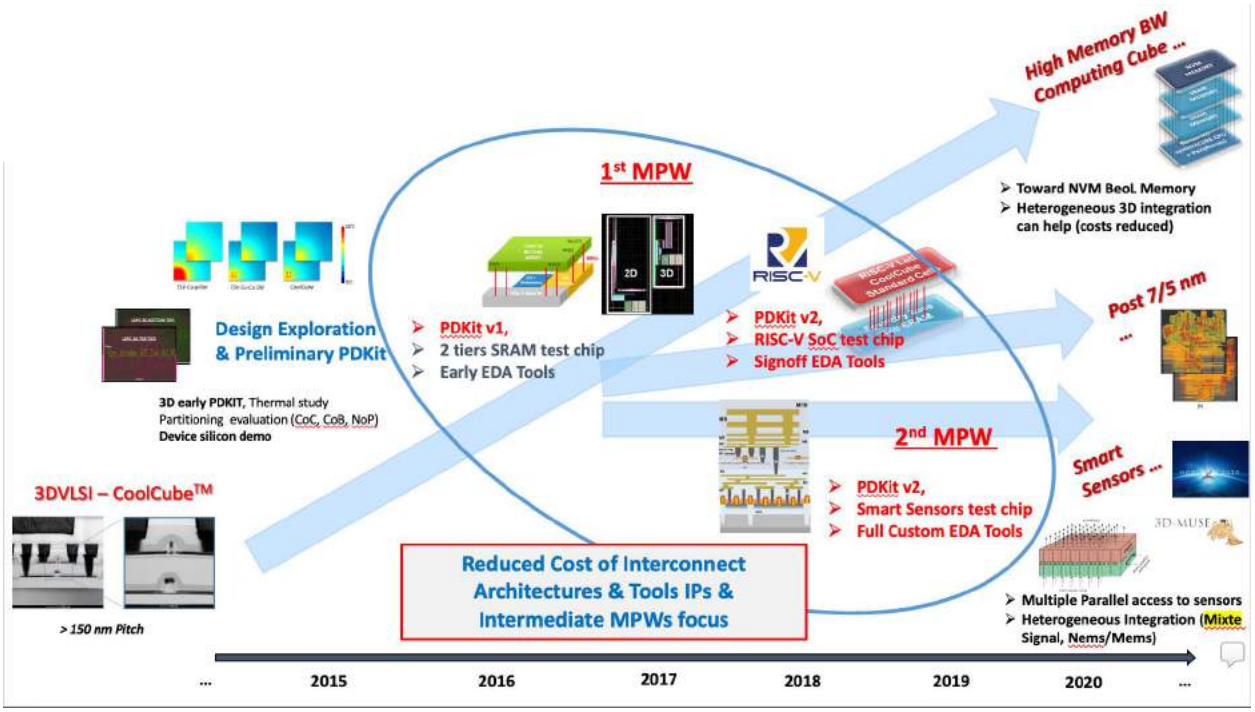

Figure 5: The 1st and 2nd MPWs resulted in the determination of the reduced cost to interconnect architectures and tools, IPs, and intermediate MPW focus

partitioning to look at the advantage of 3D compared to a 2D architecture (Figure 5).

The bottom level was dedicated to all decoding logic, drivers, I/Os, and redundancy. The top level was a 128x128 SRAM array connected by MIVs. Three scribe lines have been designed, including a 2D reference 16kb SRAM with 32-word redundancy blocks, and two 3D 16kb SRAM with 32-word redundancy block either using MIVs or single 3D TSVs.

The objective will be a first tape out at IP level (building block) but early results from layout show a 40% footprint reduction, with ~100000 transistors on top cold process, and 2068 MIVs – Density: 37600 MIVs / mm². Based on the same methodologies, a 2nd test chip resolving a 32-bit RISCV (RI5CY) SoC will be embedded in the 3D Muse MPW in order to perform a real case benchmark between 3D and 2D.

Test cases, applications, and future work

After more than ten years of research and development, Leti sees the CoolCube concept becoming a common platform for multi-application-driven technological developments. Leti's strength has been to gather a full ecosystem of partners around its program, including materials companies, tool suppliers, EDA providers, fabless and fab companies, test, and characterization support. Leti is now implementing the first application engagements in industrial product roadmaps to get the full benefit of the technology.

FOR SYSTEMS REQUIRING HIGH PERFORMANCE, ADVANCED 3D TECHNOLOGIES SUCH AS HYBRID BONDING AND MONOLITHIC 3D ARE CONSIDERED TO BE THE ONLY WAYS TO PUSH COMPUTING TO HIGHER LEVELS.

A first application of the concept will be to enable partitioning up to the transistor device scale (Figure 6). When imaging N/P or P/N FET stacking, enormous gain is obtained by boosting each FET performance independently on each level. Each FET polarity would pick up the best possible channel material, gate stack, stressors or contact metallurgy. A 3D fine connection at the device level will provide device level outperformance (current/capacitance) and will spare front-end players numerous expensive lithography steps and process selectivity challenges vs. planar 2D schemes.

This Holy Grail requires redesign of all libraries and standard cells with a limited area gain, much below 50%, considerably reducing the area gain for SRAM, for example.

Leti is also relying on a CMOS over CMOS approach as we have seen earlier. The first ideas are coming for new digital architectures including logic-on-memory for data-intensive computing (data analytics or data

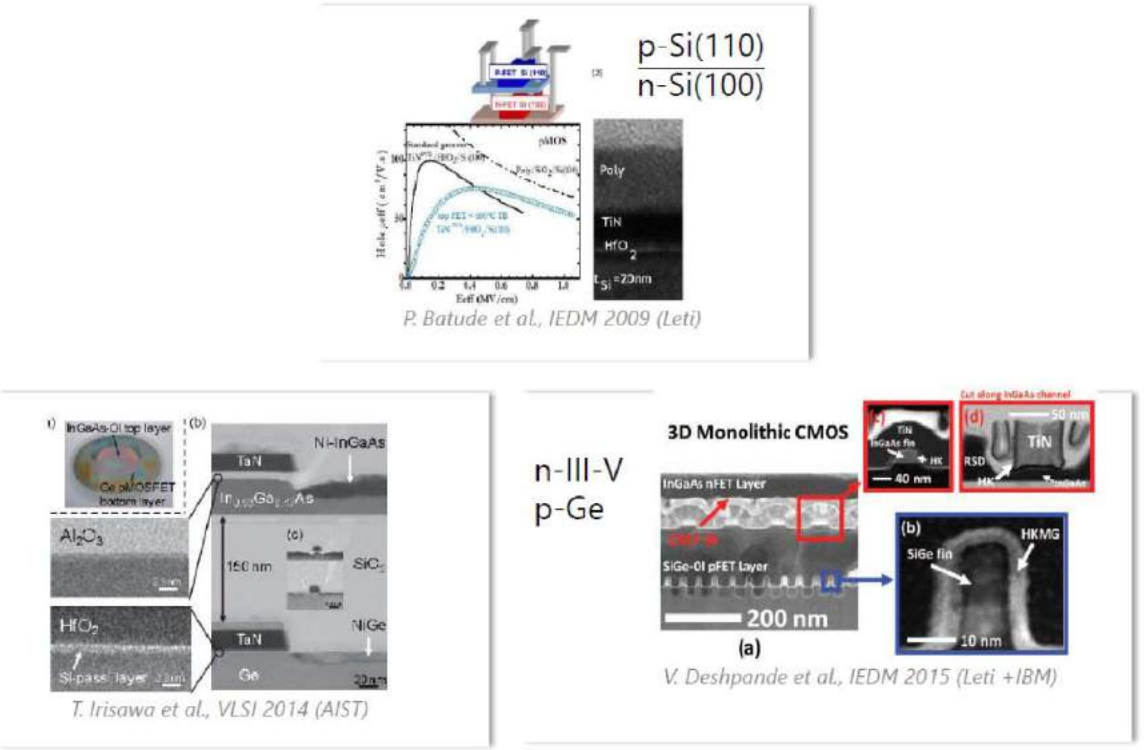

Figure 6: N/P or P/N: the integration engineer's holy grail

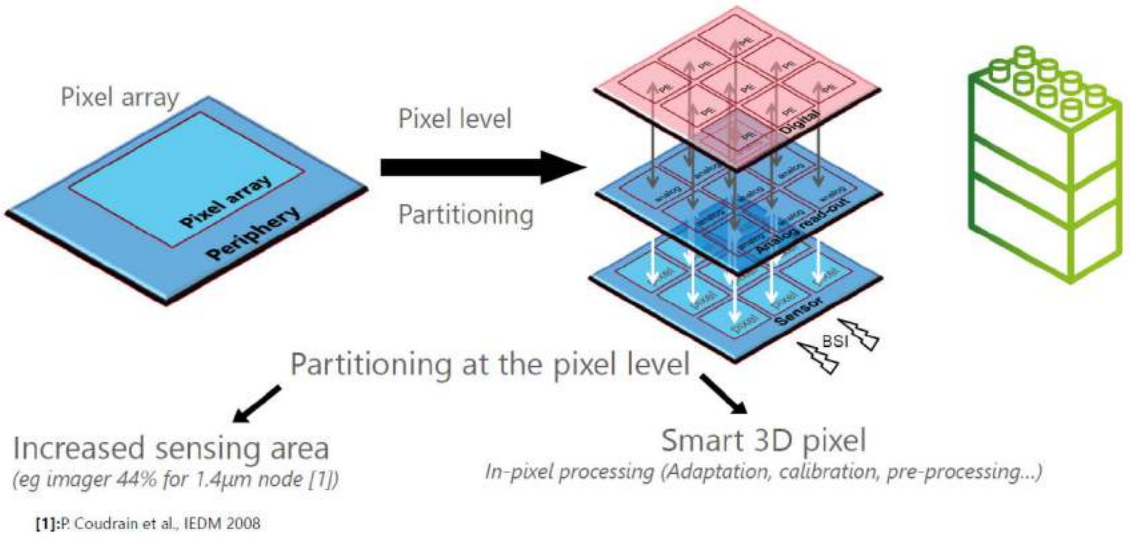

Figure 7: Smart sensing in a matrix

retrieval), and of course for neuromorphic convolutional neural networks for deep learning and artificial intelligence accelerators.

Both test cases are dominated by memory and wires, organized as a parallel matrix of computational data loading, with performance obviously enhanced by the density of contacts allowed by the CoolCube integration. It really can be seen as an extension of 3D hybrid bonding for close memory/logic entanglement and disruptive design approaches.

The first industrialization for CoolCube will probably come from smart sensing in a matrix. First applications will be driven by image sensors, µdisplay panels, NEMS mass spectroscopy, biological nanowires sensing or DNA computing.

Partitioning the application at the elementary sensing spot increases the sensing area while also permitting a smart 3D in-element processing for sensing adaptation, calibration, pre-processing, etc. CoolCube offers each sensor element to be addressed individually with more than one tiny contact, inducing less parasitic effect, better signal development and optimization between the analog and the digital stages.

Lastly, CoolCube will be one of the major enablers to allow Leti to develop a multi-thousand qubits processor in the next ten years, based on the CMOS silicon spin technology developed by the Grenoble team including CEA Leti, CEA Inac and CNRS Néel Institute. Much less advanced than the superconducting devices, silicon spin qubit reveals itself to be as performing but much more scalable thanks to VLSI 300mm process integration. Then, the only way to conceive a system architecture for a quantum processor is to use 3D technology, at a pitch density level made possible by using CoolCube 3D sequential integration.

About the Author

Jean-Eric Michallet manages the Microelectronics Components Department at CEA-Leti, covering advanced CMOS, advanced non-volatile memories, mask and PDK, models/simulations and test/characterization activities. He joined CEA-Leti in 2013 as Microelectronics Business Development Manager after a 20-year career in technical and management positions at Altis Semiconductor and IBM Microelectronics.

Prior to joining CEA-Leti, he was technology transfer officer at University of Lyon (France). He was member of the board of Manesman Business Angels, an investment network for high tech start-ups in Paris (France). Jean-Eric Michallet received the M.S degree in Microelectronics from ENSERG Institute (Institut National polytechnique de Grenoble, France), an Executive MBA and a Master's degree in International Management from Dauphine University Paris (France)/ UQAM Montreal (Canada) and a Management Certificate, Sustainability and Social Responsiveness from ESDES Lyon.

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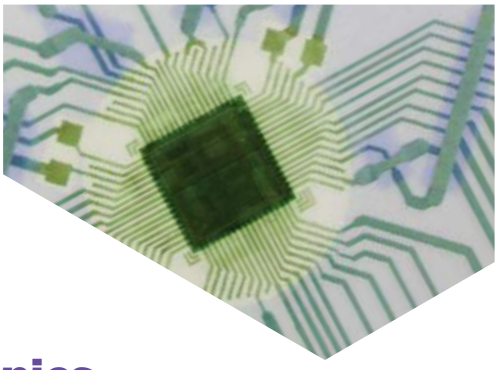

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Addressing the Challenges of Surface Preparation for Advanced Wafer Level Packaging

An interview with Anil Vijayendran, Veeco Instruments

As the semiconductor industry shifts focus from CMOS scaling to heterogeneous integration, the importance of surface preparation and wafer cleans during semiconductor device manufacturing is migrating from front-end wafer processing to back-end wafer level packaging processes. This is due to a combination of high-reliability applications, such as autonomous vehicles, 5G, artificial intelligence (AI), and the internet of things (IoT), and the high-density requirements of the advanced packaging technologies being used. For higher density fan-out wafer level packages (FOWLP), 2.5D and 3D integration technologies, proper preparation of the wafer surface, and ongoing clean steps throughout the process flow, can greatly impact the reliability of the device for which that chip package is destined.

To get a clearer picture of how this impacts semiconductor equipment and materials suppliers, 3DInCites spoke with Anil Vijayendran, vice president of marketing at Veeco Instruments, Precision Surface Processing Division.

3D InCites: What do you see as the major trends in the advanced packaging space, especially in the context of surface preparation methods over the last 10 years?

Vijayendran: During this time the industry has seen a push toward wafer-level packaging (WLP) to meet growing performance demands in input/output (I/O) density, speed, form factor. Starting in 2009, the earliest form of fan-out wafer level packaging (FOWLP) was put into production. Now, more designs are being introduced by outsourced semiconductor assembly and test (OSAT) providers and foundries to address a growing application base.

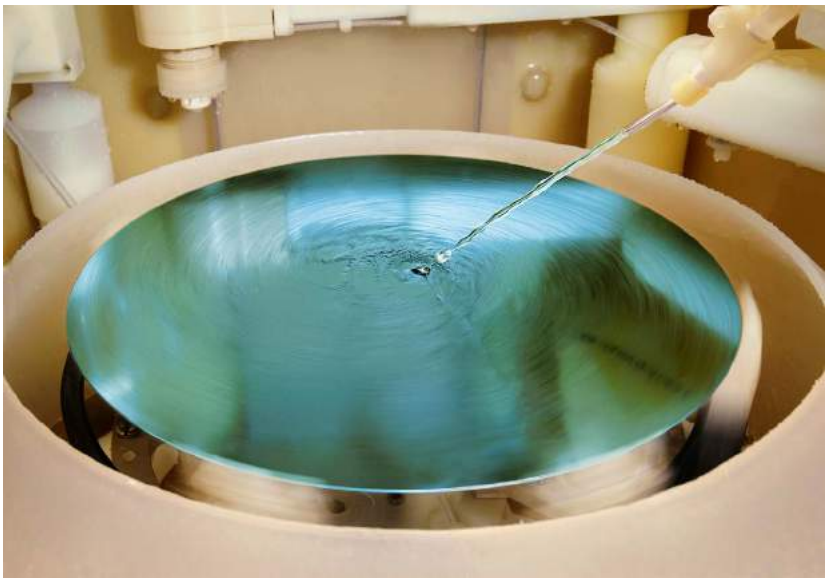
WLP requires a higher degree of control and process capability to maintain superior yields. From a surface preparation perspective, there are more cleaning steps with a greater attention to defectivity. Specific to wet processing, the last 10 years has seen a greater number of strip, wet etch, and plating steps with a greater focus on dimensional control as this packaging method has become more prevalent.

A key challenge to the adoption of WLP is cost. As such, suppliers have been tasked with working closely with fabs to meet the technical requirements of evolving packaging designs while still driving lower cost-of-ownership. This partnership is dependent on refined hardware, chemistry and process to achieve sustainable high-volume manufacturing (HVM) results. Over the past decade, we have also seen increased focus on environmental health and safety (EHS) by decreasing adverse impacts of the chemical formulations used.

3D InCites: How have these trends affected the wet processing equipment and materials market?

Vijayendran: The equipment and materials industries have experienced significant change over the last 10 years. For example, manufacturers have relied heavily on wet benches for PR strip and etch processes. We've also seen the shift to single wafer equipment to improve process control. Wet benches, while less expensive, cannot meet the stringent uniformity and undercut requirements of advanced package techniques that single wafer equipment can. But, as mentioned before, these single wafer tools must deliver competitive CoO. This has led to a greater focus on filtration, reduced chemistry usage and chemical monitoring to minimize operational cost.

From a chemistry and materials view, the new advanced packaging methods have introduced new bumping and barrier materials – moving from traditional solder to materials such as gold, nickel, and titanium. Other shifts included transitioning from a fluxing process to a fluxless process as dimensions shrink in 2.5D and 3D packaging applications. These changes required new chemistries and methods of delivery that maintain suitable throughput and are cost competitive. Moreover, chemistry manufacturers have invested significantly to optimize formulations that improve process characteristics such as material selectivity. From an EHS



standpoint, there has also been a shift away from manually operated equipment and refinement in airflow design with wet process tools, thus reducing worker exposure by changing the tools performing the processes as opposed to changing the solvents themselves.

3D InCites: What challenges have packaging houses and equipment manufacturers and materials suppliers overcome in the last decade?

Vijayendran: A significant challenge for the industry has been to drive costs down while developing advanced technology that meets a wide range of application requirements. To overcome this hurdle, packaging players have consolidated. The trend towards fewer, but larger-sized, packaging entities allows for a greater amount of dedicated resources to focus on difficult technical problems. As these technical challenges became more complex, packaging houses continued to partner with equipment and material suppliers that can tailor solutions for their needs. This trend is especially prevalent today as larger equipment suppliers traditionally focused on front-end fabrication have receded from the advanced packaging market. Meanwhile, nimbler, mid-sized global companies and local suppliers have built product offerings dedicated to the advanced packaging market.

3D InCites: Looking forward, what technical challenges do new packaging techniques present to the wet processing market?

Vijayendran: As Moore's Law slows, and the expense of device scaling below 7nm becomes increasingly challenging, chip manufacturers are looking to heterogeneous packaging techniques to achieve the performance benefit. Heterogeneous packaging involves significant complexity such as substrate and dimensional control, which impacts wet processes. The substrate material can be severely warped (in some cases up to 10mm), so the equipment must be able to handle this deflection while still maintaining process performance. The substrate type can also change from silicon to a glass or polymer compound. Equipment must be able to handle these different materials and in many cases on the same tool. From a dimensional standpoint, as the I/O count increases, the line/space (l/s) dimensions will shrink to 2µm while the number of redistribution (RDL) layers increases. Surface processes must be able to maintain dimensional control without damaging the substrate. As an example, for a 100µm bump, a 1µm undercut has a minimal effect on performance. At 2µm l/s, a 1µm undercut will be a performance killer. Equipment and chemistry manufacturers will be pushed to provide better process control to enable these smaller dimensions moving forward.

3D InCites: What about cost reduction trends and the impact on the industry?

Vijayendran: In recent years, it has been a constant battle to maintain performance and low cost. Yet for these advanced packaging techniques to become mainstream, costs must continue to decrease. One way could be through implementation of panel-level packaging. By increasing the substrate size, manufacturers expand the usable die per substrate. On paper, this may seem like a simple concept, but it is more difficult in execution. Process performance on rectangular substrates will be different than on circular substrates. Wet processes, such as etch and clean, will not have the same uniformity on rectangular substrates as circular ones without re-thinking the equipment capability, process, and design. Difficulties with uniformity are further magnified by the sheer area of the panel as well as warpage across the panel. Handling such large substrates also poses significant challenges. Robotic systems and system architectures must be modified to handle the heavier substrate as well as the warpage. Lastly, moving all equipment suppliers to a new substrate size is of critical importance.

3D InCites: Given these challenges, what is your prediction for the wet processing equipment and materials market for the next few years?

Vijayendran: Looking ahead, we will see continued consolidation in the industry. Device manufacturers will push OSATs for more technical advances to enable further performance benefits to meet requirements for 5G, AI and the IoT. The industry will be focused on how to improve process control at 2µm l/s and below. Undercut control and defectivity will become more important as defects could now kill the package. Tools will become more flexible as the number of processes, wafer types, and sizes increase. Panel-level packaging may also gain momentum for certain devices, which could be a catalyst for a parallel investment cycle in the industry. OSATs will need the flexibility to stay competitive and continue to push suppliers to offer more modular solutions. Finally, OSATs and foundries will need to partner with more global suppliers that have design and full process support capabilities as they look to build a competitive supply of advanced packaging offerings.

About Anil Vijayendran

Anil Vijayendran is the vice president of marketing for Veeco's precision surface processing business unit. where he leads all end-to-end product management and marketing efforts.

Prior to Veeco, Vijayendran was the vice president of sales and marketing for MiaSolé, and served as the director of business development and product management at Novellus Systems, a Lam Research company. Vijayendran holds an MBA from the University of California, Berkeley, and an MS and BS in chemical engineering from MIT.

Reliable Process Control Solutions for the Growing Power Device Market

By Dr. Dario Alliata, Unity-SC

The expected increase of power device markets — and more particularly insulated-gate bipolar transistor (IGBT) products for automotive and other applications — is pushing the semiconductor industry to adopt specific process solutions. The maturity of IGBT market, boosted by a booming demand for electrified vehicles (EV) and hybrid electrified vehicles (HEV), and the consequent need for improved manufacturing yield to stay economically competitive, has forced several device makers to collaborate with their supply chain in developing ad-hoc process control solutions.

For several years, Unity-SC has collaborated with major IGBT makers to secure the most critical fabrication steps in the manufacturing chain from the front-end down to the advanced packaging area. More specifically, the company has focused its efforts to develop non-conventional solutions for the wafer thinning area.

In fact, thanks to the reduction in wafer thickness, shorter wiring or through silicon via (TSV) pitch can be reached and simultaneously package size miniaturization targets are met, while simultaneously enhancing the device performance and reducing power loss.

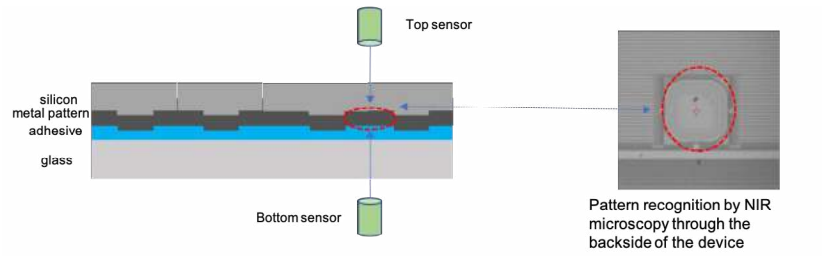


Figure 2: Simultaneous thickness measurement of a four-layer stack at gate area. From top to bottom: Silicon/metal/adhesive material/glass carrier

In the typical process flow used for IGBT fabrication, the backside thinning is identified as one of the most critical steps (Figure 1).

Back grinding is the most popular process method used to reduce the wafer thickness because it is a low-cost and high-speed technique. However, the mechanical stress and heat applied during this process generates damage that can be removed by using different methods to improve the final surface finish. Nevertheless, any remaining defect on the backside surface may generate final defective dies.

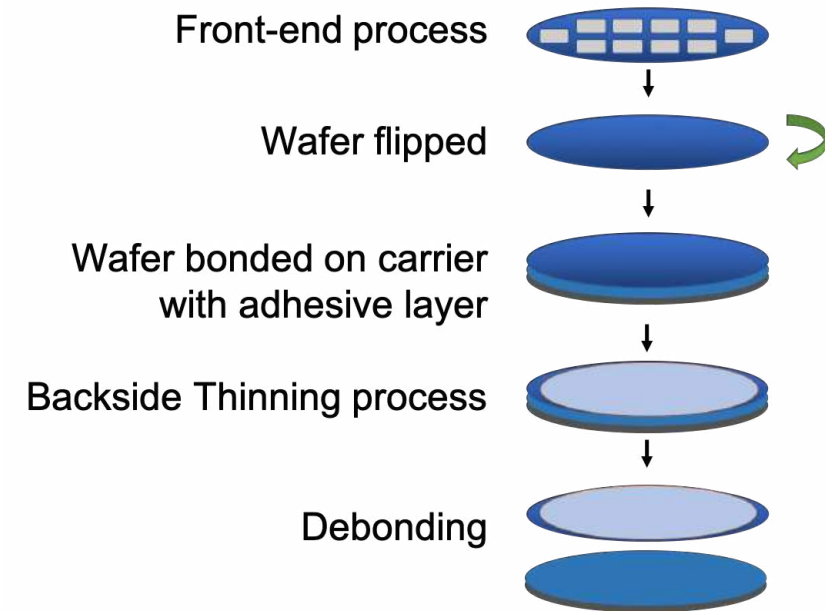


Figure 1: Fabrication process flow of IGBT device

In-line control of the device thickness and its integrity from defectivity perspective are a must to secure the product functionality and prevent future failures once in use on EV/HEV.

Thickness control

Fabrication specifications for the thickness of the final package are often connected to reliable performance. Consequently, measurement methods with good Gage repeatability and reproducibility (GR&R) at key device locations must be chosen.

In the example illustrated in Figure 2, the wafer is glued on a temporary support carrier during thinning. The thickness of four material layers is simultaneously measured by combining two interferometric point sensors that use time-domain analysis to control all layers from both sides of the structure. The integrated visual capability of the measurement sensors allows the identification of the embedded target non-visible at the surface by looking for its pattern at sub micrometer precision through the silicon with near infra-red (NIR) microscopy.

The measurement capability is reached on a stack that includes transparent material like Si or adhesive, and opaque material like metals, where thicknesses for each layer may vary from a few microns up to almost a millimeter. On a metrology tool only capable of addressing one-layer thickness at the time with a dedicated technique, this would require stopping the wafer.

Today, however, the device maker can choose metrology platforms like the TMAP Series from Unity-SC, which combines complementary technologies and an optimized optical design to address metrology control in one single step. This translates to a considerable reduction in operational cost for the device maker.

Using complementary information gathered while measuring the thickness, the TMAP series can quantify the bow/warp and the total thickness variation (TTV) of the bonded wafer and prevent the wafer from continuing through the production line if it is no longer within the specifications. This avoids wafer breakage in the fab that incurs costly equipment downtime.

Backside thinning quality control

The aggressive backside thinning process needed to reduce package size has the potential to introduce latent defects that might cause device failure even years later after its fabrication. Traditional automatic optical inspection systems are not sensitive enough to catch killer defects with very low optical contrast.

Unity-SC has developed proprietary detection technologies capable of detecting all critical anomalies. For example, phase shift deflection (PSD) is a powerful technique that guarantees detection of topographic defects in a height range of only few nanometers, and at an inspection rate of 100wph.

PSD is used to inspect the backside surface and generate complementary whole wafers images, each one used to extract different digital optic identifiers (DOIs) and wafer macro properties (Figure 3). Topographic defects like comets, surface dislocations, and star and hair cracks can be detected and separated from grinding marks through automatic defect classification (ADC) analysis of the curvature image, while stains and residues are extracted from the reflectivity image. Additional information on the wafer's global integrity are reachable from the topographic map.

Additionally, the edge of the wafer can be inspected by 2D line scan technology based on confocal chromatic imaging. The natural extended depth of focus provided by the chromatic lens is the perfect tool to recognize chips, cracks, and contamination located at the five zones of the bevel area (top, top bevel, apex, bottom bevel, bottom), that can propagate on the wafer during process stress conditions and damage the dies.

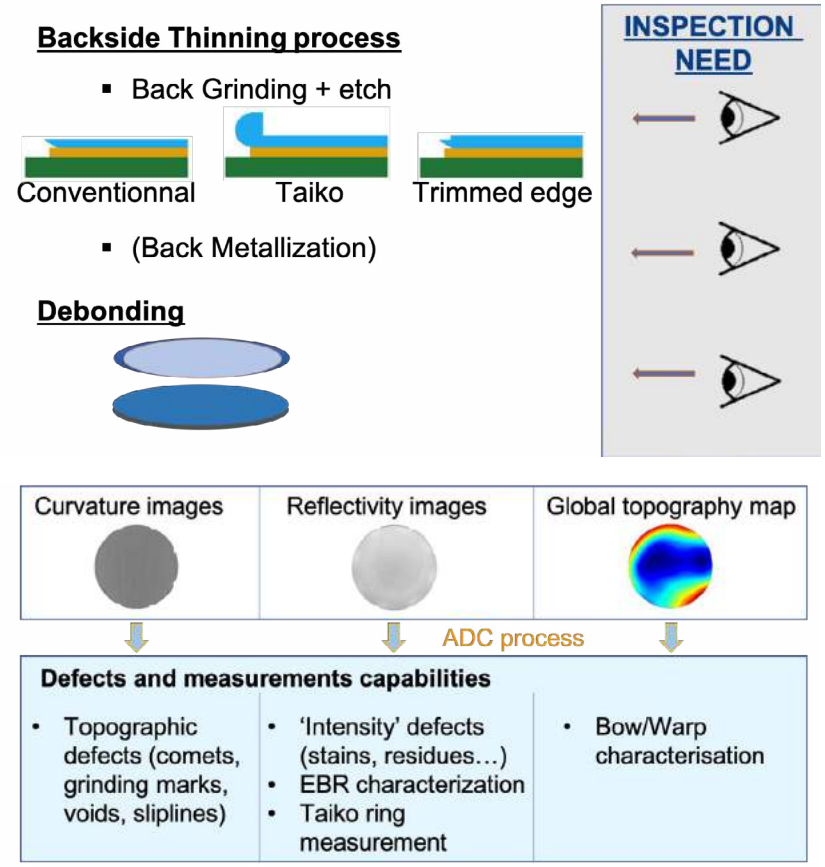


Figure 3: Quality control strategy and DOI detectable by 4SEE series from Unity-SC equipped with deflector module

Handling challenges

Beside the measurement difficulty, another major challenge is wafer handling during the thinning process. In fact, when the wafer's thickness is reduced from several hundred microns down to few tens of microns, the mechanical property of the silicon substrate prevents the wafer from being moved across multiple processing tools without ad hoc solutions. Any device maker is forced to finding the best approach to overcome the handling limitations at a sustainable cost. The wafer can be temporarily bonded on a silicon or glass carrier, it can be transformed to a Taiko wafer, or mounted on a dicing frame. Notch-detection on dirty bonded wafers and the need for partial or full contactless handling are examples of the additional capabilities faced by equipment manufacturers.

As supplier a of leading-edge inspection and metrology equipment worldwide, Unity-SC is committed to developing reliable solutions to meet any specific fab requirement. Investments in internal development, as well as mergers and acquisitions over the last two years, provides customers with the validity of our process control capabilities, and the uniqueness of our contribution to secure their fabrication processes.

Today, with several 4SEE and TMAP systems in use at IGTB makers, and thanks to bilateral collaboration with our partners, we are ready to serve almost any wafer thinning need.

3-D NAND – Where Haste You So?

By Andrew Walker, Schiltron Corp.

Sixty-four towering spires in products; Ninety-six on the verge of manufacturing and counting; Single chips with a trillion memory bits all hovering above a piece of crystalline silicon that contains the control circuitry; Deep and narrow chasms being etched and filled using tools that were "out of this world" just a few years ago; Dedicated multi-billion dollar fabrication facilities churning out millions of silicon wafers containing trillions of memory bits; And a roadmap to hundreds of layers.

That's where we are now with 3-D NAND. How did we get here so quickly? And what does the future hold for this technology?

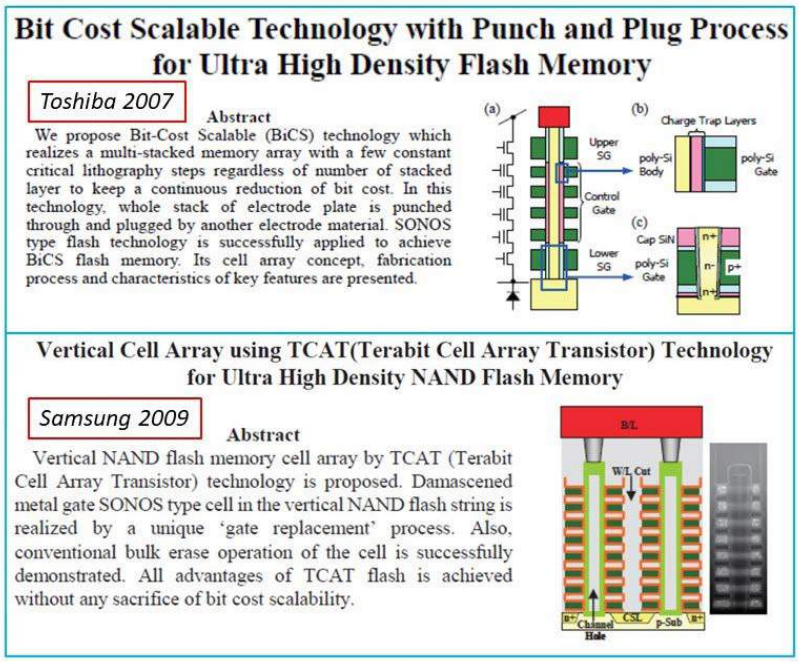
Ten years is a lifetime in silicon technology but as with all things silicon, 3-D NAND is an "evolutionary revolution". It builds on what has gone before. Nothing really "comes out of the blue". A NAND string is a NAND string whether it be in 2-D or 3-D. It is just a series connection of field-effect transistors where each one has the ability to store electric charge that changes its threshold voltage. Each building block of the technology evolved from other building blocks whose origins stretch back across decades.

Innovations that are regarded as breakthroughs at their moment of introduction meld into the increasingly complex fabric of the history of technology. Technology development drives ever onwards solving intractable problems through increasingly cross-disciplinary approaches. The rate of innovation increases almost as a corollary to Moore's Law. The history of Flash memory is a history of the semiconductor industry itself. For those who are curious, type the following into Google search: "tunneling through barriers Andy Walker".

So how did 3-D NAND get here?

At a strategic level of course, it looks fairly straightforward. The rise of "Big Data" and therefore the need for "Big Memory" coincided with 2-D NAND running out of steam. At the next level, other considerations come into play: the explosive rise of mobile applications; the need for speed to get to data; the absence of moving parts to improve reliability.

And what does "running out of steam" really mean? 2-D NAND has always been driven by lithography. Reducing the cost per bit means shrinking the memory bit. The memory bits get closer together



Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory

Toshiba 2007

Abstract

We propose Bit-Cost Scalable (BiCS) technology which realizes a multi-stacked memory array with a few constant critical lithography steps regardless of number of stacked layer to keep a continuous reduction of bit cost. In this technology, whole stack of electrode plate is punched through and plugged by another electrode material. SONOS type flash technology is successfully applied to achieve BiCS flash memory. Its cell array concept, fabrication process and characteristics of key features are presented.

Vertical Cell Array using TCAT(Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory

Samsung 2009

Abstract

Vertical NAND flash memory cell array by TCAT (Terabit Cell Array Transistor) technology is proposed. Damascened metal gate SONOS type cell in the vertical NAND flash string is realized by a unique 'gate replacement' process. Also, conventional bulk erase operation of the cell is successfully demonstrated. All advantages of TCAT flash is achieved without any sacrifice of bit cost scalability.

Figure 1 – Excerpts from the 3-D NAND papers from Toshiba in 2007 and Samsung in 2009 (© IEEE).

and increasingly electrically interfere with one another. At the same time, the amount of electric charge that each can store reduces, resulting in reliability issues. Heroic efforts are made to "keep the show on the road" and get to the next technology node. The cost of doing so increases each time with the result that the technology "brick wall" is really the gradual law of diminishing returns.

Going 3D to increase memory density was being worked on in parallel as 2D NAND was shrinking. Thin-film transistor (TFT) based 3D Flash concepts using floating gates to store charge were published in the 90s while the first charge trap TFTs using the Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) approach came out in the early 2000s. And then in 2007, Toshiba (it always seems to be Toshiba) published their seminal paper on bit-cost scalable technology. Two years later, Samsung published their version called "Terabit Cell Array Transistor". Figure 1 shows excerpts from those two papers. All versions of 3-D NAND in production today can more or less trace their heritage to these — except for Intel and Micron. These companies have favored the use of floating gates to store charge probably due to long-held engineering suspicions about the manufacturability of charge trap approaches.

What does the future hold?

The silicon memory industry has become adept at squeezing out cost in whatever technology is in development. This translates to maximizing memory bit density.

For 3D NAND, the ways to do this are:

- Stuff peripheral circuitry underneath the 3-D memory array
- Minimize lateral cell dimensions
- Maximize the number of electrical bits per cell

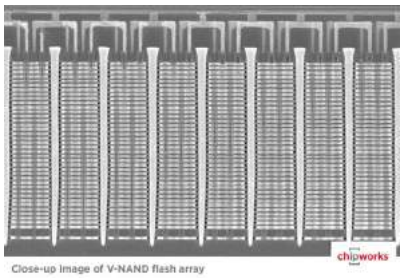


Figure 2: Cross section of Samsung 86 Gb 32-layer 2nd generation v-NAND (source: chipworks)

- Stack more layers

It looks like the first three approaches have been exhausted. Using silicon area underneath the array is obvious but tricky since low-resistance metals cannot be used because of subsequent process temperatures.

Minimizing lateral dimensions has involved sharing vertical source connections with multiple vertical strings. Maximizing electrical bits per cell has taken 3D NAND from single-level cell (SLC), through multi-level (actually two) cell (MLC) and triple-level cell (TLC), to quadruple-level cell (QLC). It looks like the only way is up with manufacturers confidently projecting roadmaps to hundreds of layers.

To make a guess at what the future holds, we need to understand what challenges stand in the way of this glittering future and what the consequences are of certain technical choices.

When more layers are added, the NAND string gets longer, its electrical resistance increases, and the electrical currents during read go down. Up until now, manufacturers have tried to minimize this effect by reducing the vertical distance between wordlines. The 3D NAND channel material is non-crystalline silicon, which has limited conductivity and exacerbates the effect. Research and development (R&D) activity is already taking place to investigate channel materials with higher conductivities. Expect to hear more discussion of this topic as it becomes critical to layer stack-ability. In addition, fancier stacking approaches may come to the fore that limit string lengths by slotting in

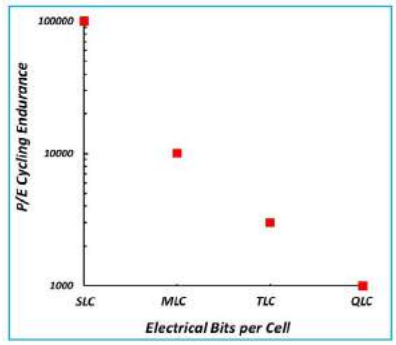


Figure 3: The effect on P/E cycling endurance of storing more electrical bits per cell. (Data from Micron at www.micron.com/products/advanced-solutions/qlc-nand).

Manufacturer	Product	Technology	Capacity (GB)	DWPD	PBW	Cell Endurance	WAF Used	Comments
Samsung	845DC PRO	V-NAND (3-D CT NAND)	400	10	7.3	27375	1.5	Nitride Charge Trap 3-D NAND
			800	10	14.6	27375	1.5	
	Z-SSD SZ985		800	30	43.8	82125	1.5	
			1600	30	87.6	82125	1.5	
			3200	30	175.2	82125	1.5	
Toshiba	PM5-M	BiCS FLASH (3-D CT NAND)	400	10	7.3	27375	1.5	
			800	10	14.6	27375	1.5	
			1600	10	29.2	27375	1.5	
			3200	10	58.4	27375	1.5	
WD (HGST)	Ultrastar SS300	3D NAND (3-D CT NAND)	400	10	7.3	27375	1.5	
			800	10	14.6	27375	1.5	
			1600	10	29.2	27375	1.5	
			3200	10	58.4	27375	1.5	
Micron	5200 MAX	3D NAND (3-D FG NAND)	240	5	2.19	13688	1.5	Floating Gate 3-D NAND
			480	5	4.38	13688	1.5	
			960	5	8.76	13688	1.5	
			1920	5	17.52	13688	1.5	
	9200 MAX		1600	3	8.8	8250	1.5	
			3200	3	17.5	8203	1.5	
			6400	3	35.1	8227	1.5	
Intel	DC P4101	3D NAND (3-D FG NAND)	256	Not stated	Not stated	Not discoverable	N/A	
	D3-S4510	3D NAND (3-D FG NAND)	240	2.1	0.9	5625	1.5	
	D3-S4510	3D NAND (3-D FG NAND)	1920	2.0	7.1	5547	1.5	
	D3-S4510	3D NAND (3-D FG NAND)	3840	1.9	13.1	5117	1.5	
	D3-S4610	3D NAND (3-D FG NAND)	480	3.4	3	9375	1.5	
	D3-S4610	3D NAND (3-D FG NAND)	960	3.4	6	9375	1.5	
	D3-S4610	3D NAND (3-D FG NAND)	1920	2.9	10	7813	1.5	
	D3-S4610	3D NAND (3-D FG NAND)	3840	3.1	22	8594	1.5	
	D3-S4610	3D NAND (3-D FG NAND)	7680	3.2	44.25	8643	1.5	
	DC P4800X	Optane (3D XPoint)	375	30	20.5	54667	1	3D XPoint
	DC P4800X	Optane (3D XPoint)	750	30	41	54667	1	
	SSD 900P	Optane (3D XPoint)	280	10	5.11	18250	1	
	SSD 905P 480	Optane (3D XPoint)	480	10	8.76	18250	1	
	SSD 905P 960	Optane (3D XPoint)	960	10	17.52	18250	1	
	SSD 905P 1500	Optane (3D XPoint)	1500	10	27.37	18247	1	

Figure 4 – Cell P/E endurances for various SSD products using either 3D NAND or 3D XPoint technology. DWPD and PBW are taken from publicly available data sheets. A WAF of 1.5 has been assumed for the NAND-based SSDs

more bitlines vertically in the stack.

Another effect of longer (taller) strings is greater disturbs on each cell during read and program. This reduces the electrical "distance" between bits in the 3-D NAND. With more than one electrical bit per cell, this distance is already limited. Expect to hear about the limits of combining TLC/QLC with the tallest 3-D NAND strings.

Finally, expect more discussion about cost, acquisition cost, total cost of ownership (TCO), market segmentation, and storage tiering. To understand why, look at Figure 2.

NAND (both 2D and 3D) has interesting limitations when it comes to cycling. The linear string of transistors means that unselected devices have to be turned on to read or program any particular cell. These actions disturb those devices. Engineering minimization of these disturbs leads to thick dielectrics in each transistor. This increases the voltages needed and the damage and inadvertent charge trapping that result from program and erase. SLC has the largest electrical distance between bits allowing more damage to build up while QLC has the least.

Manufacturers cope with this dramatic effect by segmenting the market into "read-centric", "write-centric" and "mixed" workloads. Storage tiering, where MLC and TLC/QLC NANDs are combined in a system, can also limit the program-erase (P/E) stress on the TLC/QLC parts.

Figure 2 shows the fundamental tradeoff that manufacturers are making is to lower acquisition cost ($/GB) while raising TCO ($/(PetaBytes written). Market segmentation and storage tiering are used to limit the TCO increase.

P/E endurance at system level uses terms such as drive-writes-per-day (DWPD) and peta-bytes-written (PBW). Figure 3 shows my conversions of these (taken from available data sheets) to NAND cell endurance. Apart from possible arithmetic error, the conversion depends on something called the write amplification factor (WAF). This basically means how many NAND writes are actually made at silicon level for each time the system decides to write and is inherent to the NAND architecture. My assumption for this is included. I have also included calculations for 3D XPoint systems as a comparison.

Several conclusions arise from this analysis. First, 3-D NAND remains in an endurance straitjacket when compared to other non-NAND charge trap Flash approaches, where orders of magnitude greater endurances are possible. Samsung's new "Z-NAND" is known to be SLC and is limited to below 100k cycles. Interestingly, 3D XPoint also seems to be limited to way below this value, at least for the products analyzed. This seems at odds with the original promise of 3D XPoint and may be intermediate products on the road to higher endurances.

Since "Big Data" will only get bigger, write-centric workloads will increase in volume. For these, the TCO is basically inversely proportional to the endurance. Expect more discussion about acquisition cost versus TCO especially given the inexorable rise of enterprise storage where sophisticated TCO models tend to hold sway. Also, any 3D technology that can use the 3D NAND ecosystem and can boost endurance by at least an order of magnitude could gain attention.

In summary

The towering spires of 3-D NAND have shot up. But they need to keep on shooting up to continue reducing cost per bit since all other avenues for cost reduction look to have been exhausted. Discussions will focus on channel materials, fancy 3-D integration schemes, ability to combine TLC/QLC with taller strings, and total cost of ownership. Interesting times indeed.

Historical Perspective continued from 14

chips with several functions on them can be "disaggregated" or "disintegrated" into separate functions. These separated functions can be fabricated at different scaling nodes to optimize final performance and reintegrated onto a 2.5D silicon interposer. This strategy also allows for IP reuse of such known good chiplets in other designs.

The current DoD DARPA program, Common Heterogeneous Integration, and IP Reuse Strategies (CHIPS), is attempting to standardize communication interfaces and physical sizes to allow for proliferation of this technology into both the commercial and military worlds.

In fact, Intel, a leading member of the CHIPS program, recently indicated that starting in 2019 it will separate various processor components into smaller chiplets, each of which can be manufactured using an optimum (performance/cost) production node. Thus, Intel could deliver "10nm CPUs", which could have 14nm and 22nm chiplet modules within them. So, memory, graphics, power regulation, and AI function could all constitute separate chiplets, some of which could be stacked with TSVs to a high-density silicon interposer.

What does the future hold?

With an end coming to CMOS scaling, something new will be taking its place. It is not clear what that new technology will be, but it is certain that it will take more than a decade to implement. The new technology will ultimately determine where packaging will go, but at this point we can only all guess what that will be. But, one thing we can say about chip packaging is, "we've come a long way baby!"

About the Author

Dr. Phil Garrou is a subject matter expert for DARPA and runs his consulting company Microelectronic Consultants of NC in the RTP NC area. He retired from Dow Chemical in 2004 as Global Director of Technology for their Advanced Electronic Materials business unit. Phil has served as Technical VP and President of both IEEE EPS and IMAPS and is a Fellow of both organizations. He has edited several microelectronic texts including McGraw Hill's "Multichip Module Handbook" and Wiley VCH's "Handbook of 3D Integration". He has won the Milton Kiver Award for Excellence in Electronic Packaging (1994); the Fraunhofer International Adv. Packaging Award (2002); the IEEE CPMT Sustained Technical Achievement Award (2007) , the IMAPS Ashman Award (2000) and most recently the American Chemical Society Award for Team Innovation (2017). His weekly publication Insights From the Leading Edge (IFTLE) has been a weekly advanced packaging blog since 2010.

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THE FIRST DECADE IN PICTURES

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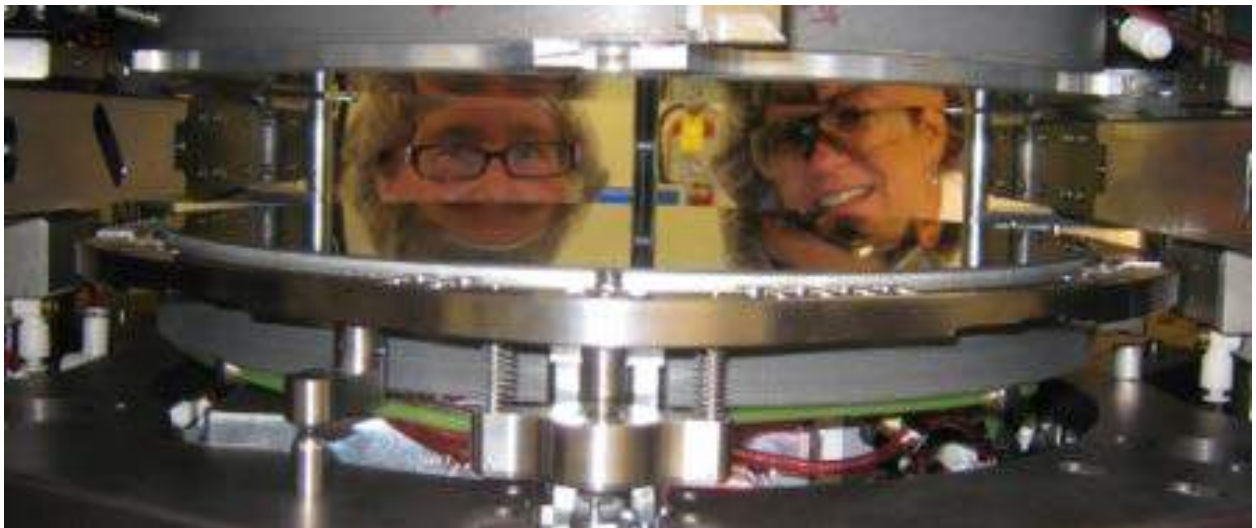

2010

2011

2012


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2013


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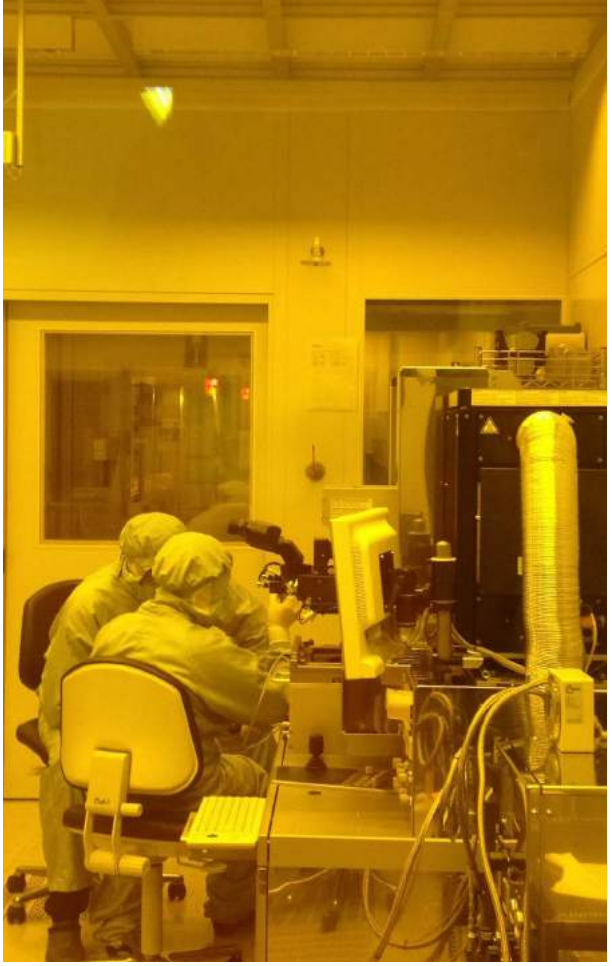

2014


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2015

2016


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How it All Began:
Even the Magic 8 Ball couldn't have called it

In my last editorial as managing editor of Advanced Packaging magazine, I suggested we should turn to the Magic 8 Ball to predict the rebound of the semiconductor manufacturing industry. But even my trusty 8 Ball couldn't have predicted my fate a week later, when the decision was made to integrate Advanced Packaging into Solid State Technology. However, as I've been told by many pioneers of emerging technology in the semiconductor manufacturing industry, a down-turn in the economy is a great time to innovate. Thus the launch of this Blog. After all, career innovations count, don't they?

My final curtain call was an interview with Replisaurus CEO, Jim Quinn and CTO, Mike Thompson, who talked about how the company is in a great position to hit the ground running when the economy rebounds. Their big news was that it's subsidiary, Smart Equipment Technology (S.E.T) will collaborate with IMEC to develop die pick-and-place and bonding processes for 3D chip integration using S.E.T.'s flip chip bonder equipment. This will invariably open doors for the start-up's proprietary technology, electrochemical replication process (ECPR).

So that's the type of content readers can expect to find on this blog. After all, industry innovators without deep pockets for advertisng still need to get the word out about their progress. The success of this industry rests on the shoulders of such companies. I'm happy to do what I can to give them a leg up.
F.v.T.

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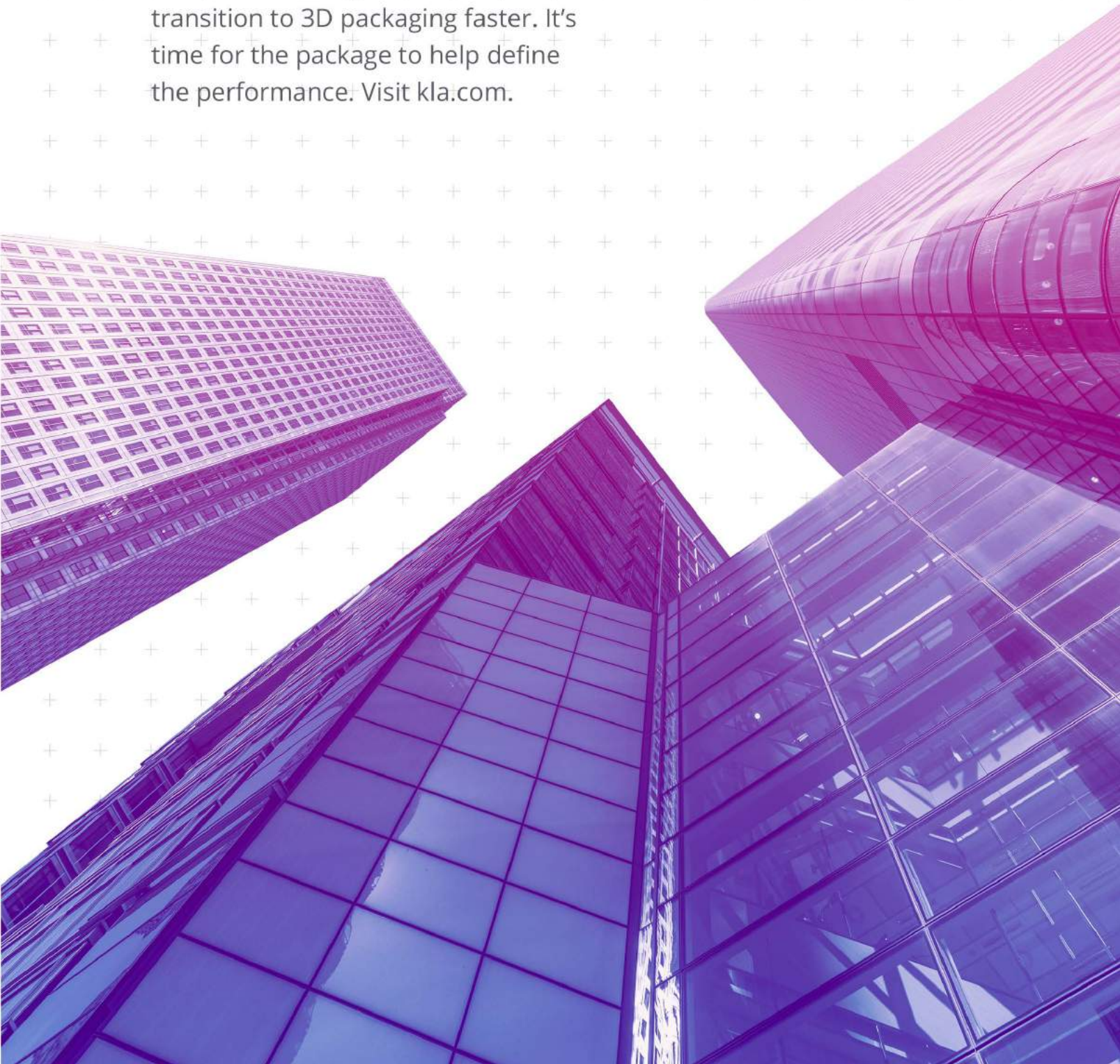

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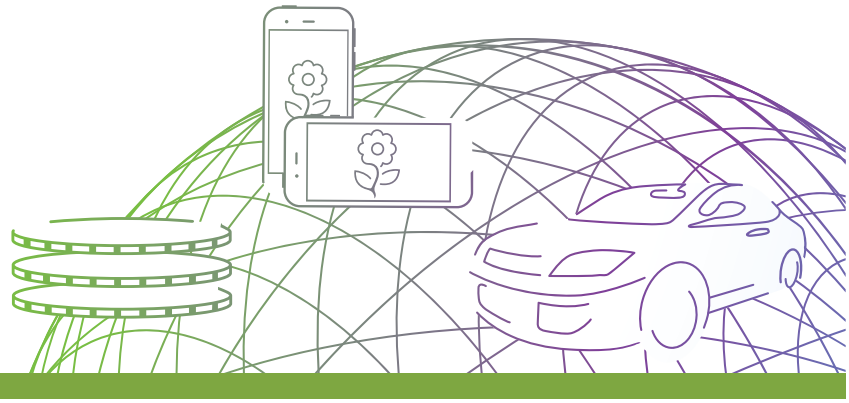

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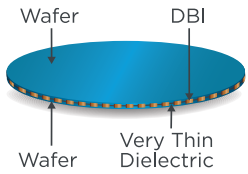

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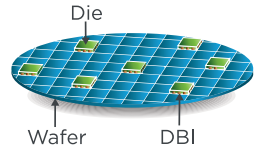
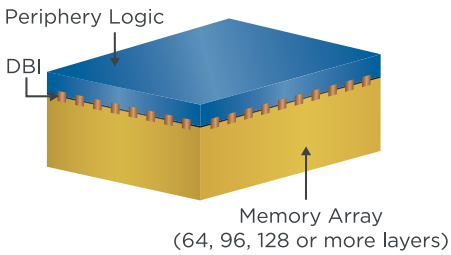


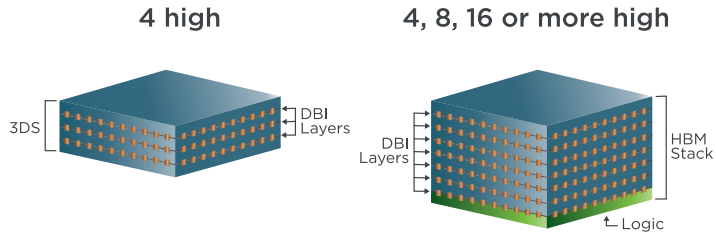
Stacked 3D NAND with DBI



Benefits

- Periphery logic & memory array segregation – optimized manufacturing processes
- High Speed 3D NAND I/O performance, similar to DDR4 DRAM
- Faster product development and shortened manufacturing cycle time accelerates time to market

Stacked 3D DRAM with DBI



Benefits

- One stacking solution for all DRAM products
- 16 high stack can meet JEDEC HBM3 height specification
- Better performance, higher bandwidth
- Lower cost, lower profile, lower power & higher reliability

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